Performance Testing of the CMS Cathode Strip Chambers

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Abstract

The production, installation, and testing of 468 cathode strip chambers for the endcap muon system of the CMS experiment played a critical role in the preparation of the endcap muon system for the final commissioning. Common testing procedures and sets of standard equipment were used at 5 international assembly centers. The chambers were then thoroughly retested after shipment to CERN. Final testing was performed after chamber installation on the steel disks in the CMS detector assembly building. The structure of the detector quality control procedure is presented along with the results of chamber performance validation tests.

1. Introduction

Cathode strip chamber (CSC) technology [1] was chosen as the baseline for the endcap muon (EMU) system of the Compact Muon Solenoid (CMS) detector [2] at the Large Hadron Collider (LHC). Multilayer proportional chambers of trapezoidal shape, with cathode strips running radially and wires stretched across the strips, was considered to be the best realization of the CSC technique for the EMU system. The cathode strips give a precise measurement of the azimuthal coordinate of the muon hits, while the anode wires give precise timing information for tagging the bunch crossing and moderate-resolution radial positions of the muon hits. The trigger part of the front-end electronics of the CSCs also provides sufficient muon hit spatial resolution and timing information for the Level-1 trigger of CMS.

The chambers are filled with a gas mixture of 40%Ar–50%CO_2–10%CF_4 at atmospheric pressure. The nominal operational voltage of 3600 V provides a gas gain of about $7x10^4$ [3,4]. No noticeable changes in the chamber gas gain or efficiency were observed with this gas mixture during the “aging” tests [5], during which the accumulated charge was about equal to the expected charge that would be deposited during 50 years of LHC operation at full luminosity.

The descoped version of the EMU detector consists of 468 six-layer CSCs currently installed on the endcap disks (the original design consisted of 540 chambers). They are arranged in 4 stations of concentric rings in both endcaps (Fig. 1). Seven different types of CSCs are used in the system, designated as ME1/1, ME1/2, ME1/3, ME2/1, ME3/1, M4/1, and ME234/2, where the first number stands for a station and the second for a ring within a station. All chambers except ME1/1 are of a similar design—they differ only by size. The special design of ME1/1 is dictated by the strong, non-uniform magnetic field and the high level of radiation expected at their location.

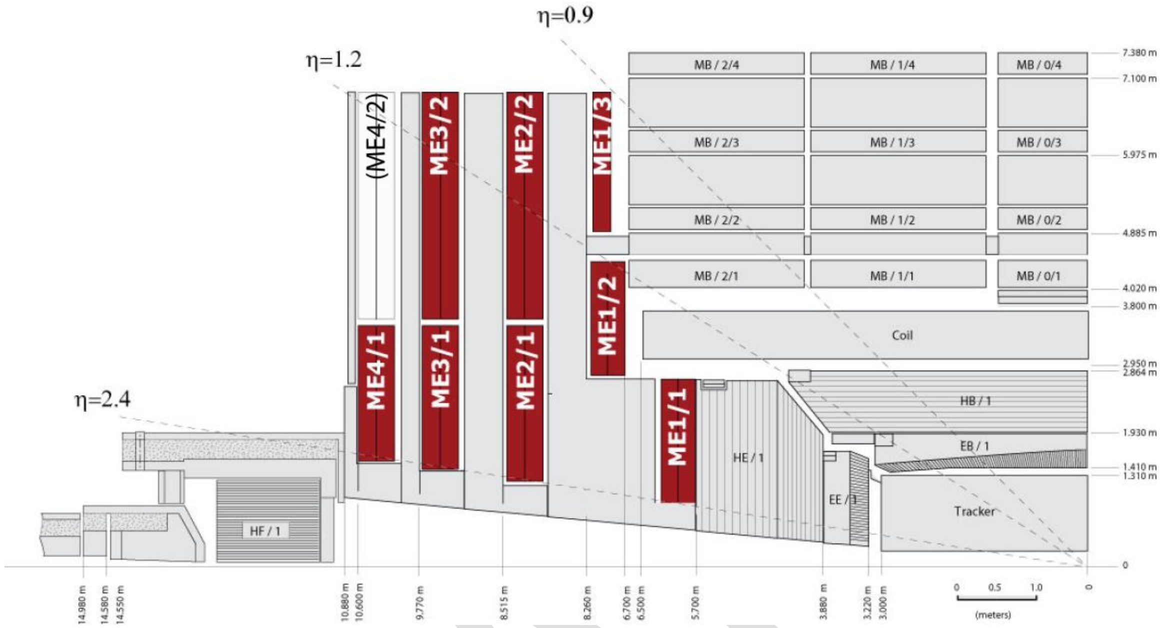

Fig.1. Cross-sectional view of the one quadrant of the CMS detector.

The construction of the CSCs was shared among Fermi National Accelerator Laboratory (FNAL) in the US (constructed 150 ME234/2 chambers), Petersburg Nuclear Physics Institute (PNPI) in Russia (36 ME2/1, 36 ME3/1, and 36 ME4/1 chambers), Institute of High Energy Physics (IHEP) in Beijing, China (72 ME1/2 and 72 ME1/3 chambers), and Joint Institute for Nuclear Research (JINR) in Dubna, Russia (72 ME1/1 chambers). The chambers built in the US were installed with on-chamber electronics at the University of Florida in Gainesville and at the University of California, Los Angeles.

The large scale of the system (almost 2.32 million anode wires, 183 168 anode, and 217 728 cathode readout channels) and the inaccessibility of the CSCs during the LHC operation demand a high level of reliability. To accomplish that goal, an elaborate quality control procedure was implemented in a standard way for all production and testing at so-called Final Assembly and System Testing (FAST) sites. Each site was instrumented with identical equipment, including a cosmic ray stand and a complete data acquisition system with unified hardware. The software used for chamber testing was distributed among the FAST sites with a complete set of documentation and step-by-step instructions.

The first comprehensive test of the chambers was done at the production FAST sites. The second stage of quality control was performed upon chamber arrival at the "test-only" FAST site located in the former Intersecting Storage Rings (ISR) collider at CERN. The final commissioning was carried out after the chambers had been installed on the steel disks of CMS. Every assembly and testing action was thoroughly documented. For this purpose, each site used the central CERN database, which contains chronological tracking of inventory information for the chambers, on-chamber electronics, and all testing results.

In this article the procedure for CSC testing is described and the results of the CSC performance validation tests are presented.

2. Cathode Strip Chamber Design

Each CSC is built from commercially made copper-clad honeycomb panels cut into a trapezoidal shape [2]. A stack of 7 panels, separated by 9.5-mm-wide FR-4 ("Flame Retardant 4" circuit board material) bars glued on the edges of every other panel, creates 6 independent gas gaps (planes) each between 2 copper cathode surfaces (Fig. 2). The stack is secured with bolts through the panels around the chamber perimeter. Gas tightness is provided by assembling the chamber with o-rings around bolts and room-temperature vulcanizing (RTV) silicone sealant that is applied to the perimeter of the contact area of the spacer bars and the panels. Operation gas flows in a zigzag path from the first plane to the last one through holes made in the panels.

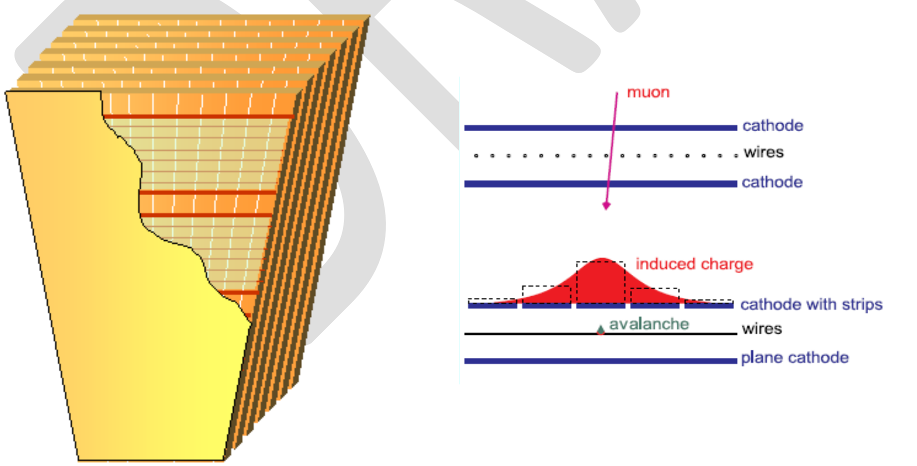

Fig. 2. CSC cross-section and principle of operation.

One of the 2 cathodes in each plane is divided into strips milled radially along the longer dimension, with the width of each strip increasing along the radius. To achieve improved spatial resolution from a 6-layer chamber, strips in adjacent planes are staggered by ½ of a strip width. The ME1/2, ME2/1, ME3/1, ME4/1, and ME234/2 chambers have 80 strips in each plane, while the ME1/3 chamber has 64 strips. The 50-µm gold-plated tungsten-rhenium anode wires are strung across the strips with a tension of 250 g and pitch of 3.1 mm. The ME1/1 chambers are somewhat different [6]: the sensitive area of each plane is divided into 2 parts with different numbers of strips. The narrow part, which covers 1/3 of the total chamber length, has 48 strips. They are currently ganged in 16 readout channels. The remaining part has 64 strips, which are connected to individual readouts. The chambers' 30-µm-diameter anode wires are stretched at about 29º relative to the base of the chamber (for Lorentz angle compensation of the primary electron drift [7]) with a tension of 80 g and pitch of 2.5 mm.

Depending on the chamber type, the anode wires are grouped together into segments with widths ranging from 2 to 5 cm. High Voltage (HV) is distributed to the wire groups on one end, while signals are readout on the other through 1-nF blocking capacitors.

The wire groups of each plane are combined into several HV sectors allowing for independent operation: 3 for the small chambers (ME1/2, ME1/3, ME2/1, ME3/1, and ME4/1) and 5 for the large ones (ME234/2). The sectors were separated by removing 6 wires between them and replacing border wires with 200-µm-thick gold plated Cu-Be ones. Each sector is connected to an individual HV power supply channel. Due to the relatively small size of the ME1/1 chambers, their planes have no HV segmentation.

3. CSC Testing

Tests of the CSCs began with a check of HV connectivity and for possible broken wires. Then the chambers were pressurized to 7.5 mbar with Ar to perform a gas leak test. During the test, the pressure inside the detector, atmospheric pressure, and temperature were monitored for 24 h. The gas leak rate was required to be less than 10^{-5} chamber volume per minute, which corresponds to 1 and 2 cc/min for the small and large chambers, respectively. If the gas leak rate exceeded specifications, leaks were identified and repaired.

The next step in the CSC quality control test sequence was a long term HV test. The chambers were flushed with working gas mixture and held for 1 month under 3 sequential HV values corresponding to the beginning, middle point, and end of the efficiency plateau. No noticeable change in measured current, which was usually less than 100 nA, was observed compared to the initial HV tests at the production sites. However, a short-term increase in leak current was observed. We regard this as part of the chamber HV training procedure. Only a few chambers did not pass the test, and had to be opened to remove pieces of wire left inside, or in one case, replace a cracked high voltage resistor.

CSC gas gain uniformity measurements completed the set of tests. Leakage currents were measured per plane at 3.6 kV with a 20-μCi Co^{60} radioactive gamma source moving on the chamber surface. Histograms of the induced current variation in the planes of the big chambers (Fig. 3), which are the most vulnerable in terms of flatness uniformity, show that the gas gain variation across a plane was typically less than a factor of 2. The greatest gas gain non-uniformity was observed for the top plane of the CSCs at the wide end. This is related to the peculiarities of the chamber assembly procedure. However, for some chambers the gas gain variation was larger than a factor of 4. When such problem was encountered in 2 planes, the chamber frame assembly was partially taken apart and the shims, which define the flatness of the chamber (the uniformity of the load on the honeycomb panels), were reexamined and adjusted to improve the chamber's flatness.

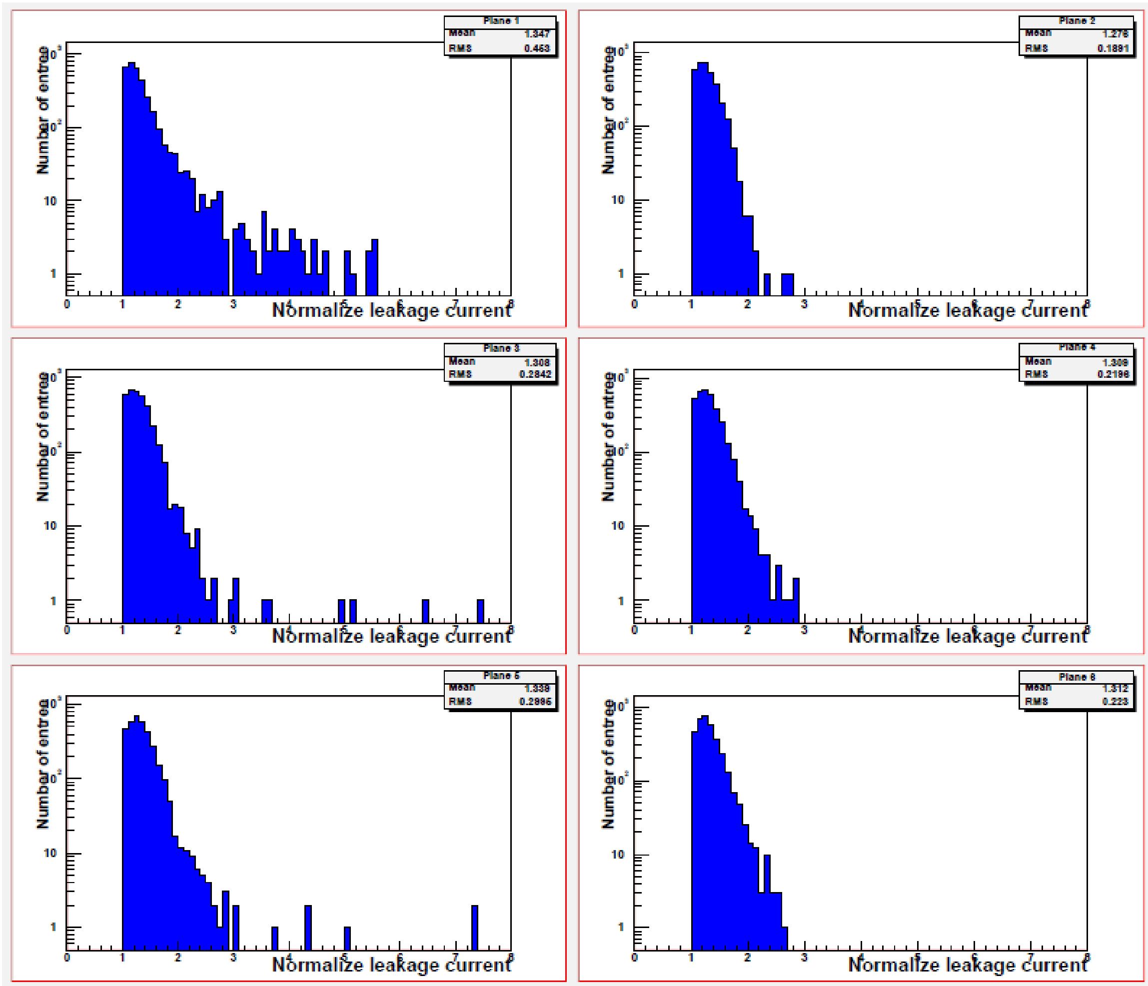

Fig. 3. Leakage current variation in the planes of the ME234/2 CSCs. The results were normalized to the smallest current in a plane.

4. CSC performance validation tests

4.1 Assembly with on-chamber electronics

The CSC on-chamber electronics consists of anode front-end boards (AFEB), cathode front-end boards (CFEB), and an anode local-charged track trigger board (ALCT) that generates muon trigger primitives for the Level-1 trigger system based on wire hit information (Fig. 4). A low voltage distribution board (LVDB) delivers the voltages necessary for the on-chamber electronics. The CFEBs, ALCT, and LVDB are mounted with good thermal contact on a copper cooling plate, which is attached on the front surface of the chamber. The cooling plate is cooled with a pressurized water system. The CFEBs are mounted as close as possible to the output strip connectors and attached to them with short input cables. The AFEBs are attached to the side of the CSC and connected to the ALCT by cables. The raw data and the trigger information from the CFEBs and the ALCT board are sent by skew-clear cables to a data acquisition motherboard (DMB) and a trigger mother board (TMB), which are located in a peripheral VME crate. Monitoring information about the output voltages and currents of the LVDB is provided by a low voltage mezzanine board (LVMB), which is mounted on the LVDB and sends the data to the DMB.

4.2 Cosmic-ray stand, trigger, readout electronics, and software

Tests of the chamber and on-chamber electronics performance were carried out on a cosmic-ray stand. The chamber was placed between 2 scintillation counter hodoscopes and connected to the data acquisition system (FAST DAQ). The hodoscopes were displaced horizontally relative to each other to enrich the trigger events with inclined muons similar to what is expected in the CMS detector. The light produced in the scintillator bars by cosmic-ray particles was collected by photomultiplier tubes from both ends. A coincidence of the 2 scintillator layers above and below the CSC provided the cosmic-ray particle trigger with a reference time of about 2 ns.

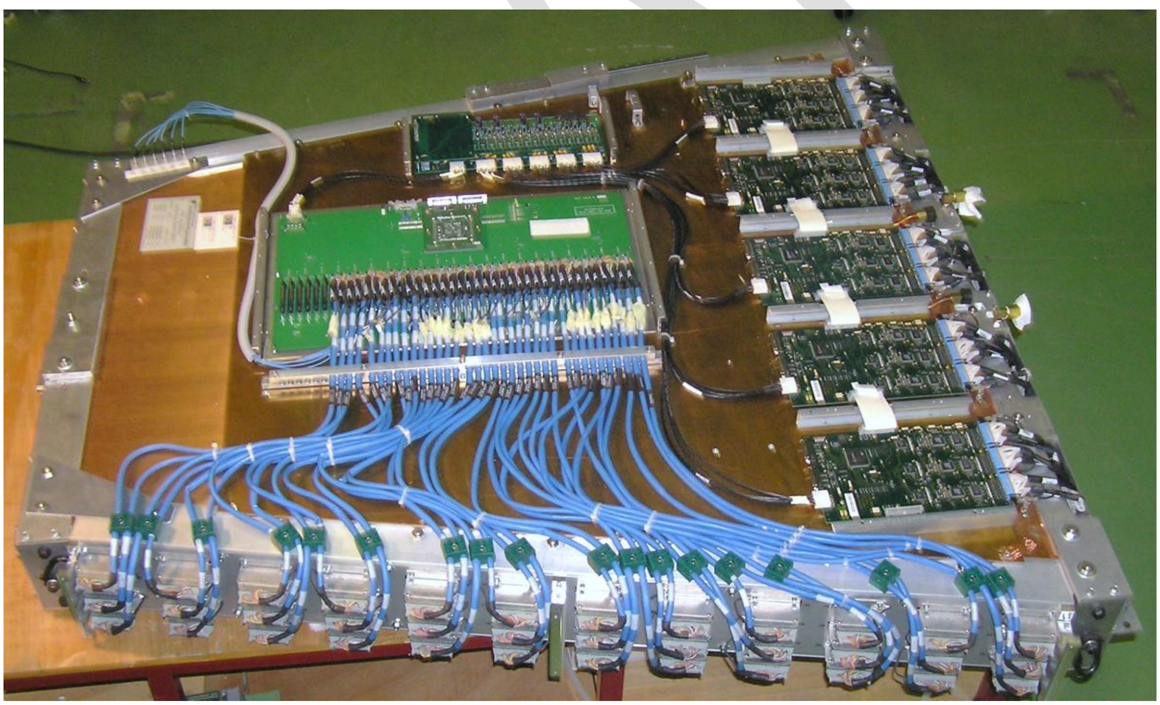

Fig. 4. Assembled ME2/1 chamber showing on-chamber electronics.

The readout electronics used the final preproduction version of the DMB and the TMB. The VME clock distribution and control board (CCB) generated the necessary test pulse signals and provided and distributed the 40-MHz clock and a final Level-1 accept trigger. Raw data were readout from the DMB through a PC Gbit Ethernet card. Communication with the VME crate was carried out by a 68360-based 3U VME bus communication controller card (Dynatem). Information about the scintillator counter hits was also readout from the discriminators.

Five different types of triggers were used in the DAQ system: the triggers related to (1) anode or (2) cathode intrinsic test pulse signals, (3) chamber self-triggers based on anode or (4) cathode hit information, and (5) triggers generated by the scintillator counter hodoscopes. DAQ test software automatically produced about 100 plots, histograms, and result files for each chamber. Information about test results and problems was shared between FAST sites by publishing the test result files and problem reports on the Web.

4.3 On-chamber electronics tests

Testing of the on-chamber electronics began with a check of the functionality of the low voltage distribution system. The control of the 19 voltage supply lines and corresponding voltages and currents were checked. The measured values were compared with limits that were set in advance for each type of CSC. The temperatures of the CFEBs and ALCT were also monitored. Then the communication with slow control parts of the anode and cathode electronics and their functionality was verified. The ADC readings of the reference voltage for the intrinsic CFEB test pulse and the comparator thresholds were checked over the whole dynamic range. When a problem was encountered, the board or cable responsible for the trouble was replaced and repaired if possible. About 6% of originally installed LVDBs and 4% of the LVMBs have been replaced.

4.3.1 Tests of anode wire electronics

An anode front-end board has one 16-channel ASIC: an amplifier combined with a constant-fraction discriminator that has 30-ns shaping time, 8-mV/fC sensitivity, 1.5-fC noise at 150-pF wire group capacitance, and a tunable threshold nominally set at 20 fC. The AFEBs were checked and certified on a quality control stand [8], where the most critical parameters of individual channels such as the input capacitor value for a test pulse and the gain were carefully measured and stored into the CMS database. Testing of the anode wire electronics started with measuring the thresholds and analog noise of individual channels. Calibrated test pulses of 30 and 50 fC were generated by the ALCT and injected into the inputs of AFEB amplifiers. For each test pulse a scan over the AFEB thresholds was made. An example of AFEB channel efficiency versus applied threshold for the 30 fC test pulse is shown in Fig. 5. The efficiency was fitted by complementary error function (**erfc**). The DAC value with 50% channel efficiency was regarded as the threshold corresponding to the injected charge.

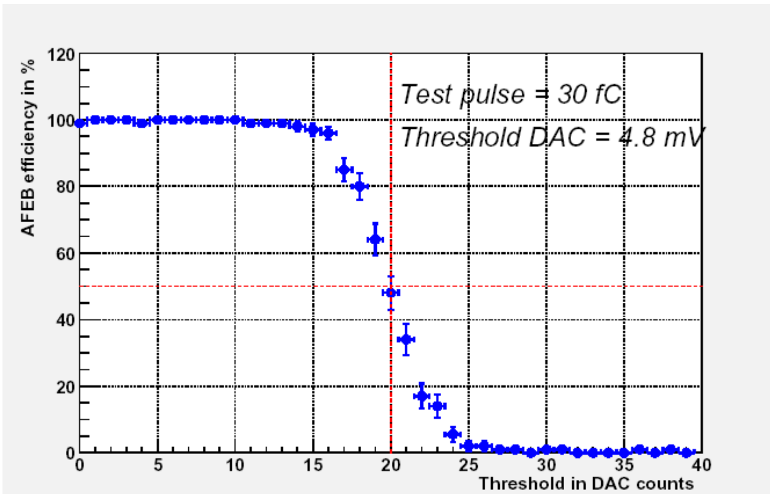

Fig. 5. AFEB channel efficiency for 30 fC test pulse versus applied threshold.

The channel analog noise is defined by the sharpness of the turn-off curve. The nominal thresholds corresponding to 20-fC signals were found by a linear extrapolation of the thresholds found for 30- and 50-fC signals versus DAC values. Since the 16 channels of 1 AFEB use a common threshold, the threshold variation among channels and their offsets and slopes were carefully monitored. Fewer than 10 boards were replaced because of an unacceptable noise level or a threshold offset.

The test of wire group connectivity and correct AFEB-ALCT cabling was performed at nominal AFEB thresholds by sending the test pulse sequentially to the test strips of each plane of the chamber. The test pulse amplitude was adjusted for each type of CSC to induce a signal of about 60 fC at the inputs of the AFEBs. The efficiency of the channel response and the plane-to-plane crosstalk were monitored. An AFEB with a near-plane crosstalk higher than 5% was rejected. A total of about 0.2% of AFEBs did not pass the test, mainly due to crosstalk from a single channel.

The propagation time for wire group signals to reach the ALCT has a spread due to differences among the AFEB-ALCT cable lengths and the AFEB average time responses. To equalize the arrival times of the anode raw hits at the ALCT within 1

CSC, a set of control delay chips are used as input circuits to the ALCT. The individual delays can be set in a range between 0 and 32 ns in 2-ns steps. The slopes and offsets of individual delays were measured in a dedicated test. Intrinsic AFEB test pulses asynchronous with the 40-MHz clock were used to make a scan over the full range of the delays. The spread of the 16 delays of each chip was monitored. No deviation greater than 4 ns from the average offset was allowed for any channel.

AFEB testing was impossible without properly working ALCTs. Various aspects of ALCT functionality were also checked during the AFEB tests. About 6% of the ALCTs were rejected at this stage of quality control.

4.3.2 Tests of the cathode strip electronics

The cathode front-end boards are comprised of an amplifier chip, comparator circuitry for half-strip position resolution, and waveform digitizing circuits (Fig. 6). The “Buckeye” amplifier chip [9] has 100-ns shaping time and 1-mV/fC linear sensitivity up to 1 V. The equivalent noise level at the nominal strip capacitance of 300 pF is typically 1.5–2 fC. The outputs are split into 2 pathways. One goes to the comparator ASIC chip, which identifies the position of muon hit at the trigger level with a half-strip resolution. The other pathway leads to the switched capacitor array (SCA) ASIC chip, a randomly-addressable analog memory chip that samples the signal waveform every 50 ns and stores these analog data for readout. During the readout cycle, 8 consecutive time bins are digitized and the SCA information is sent to the DMB.

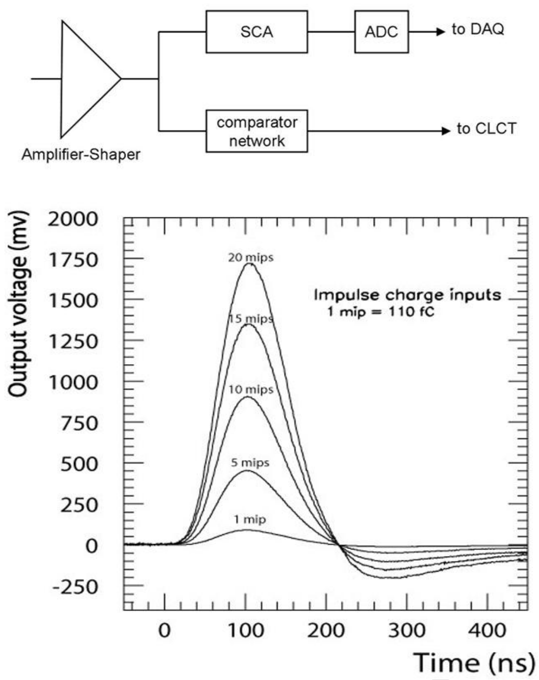

Fig. 6. Diagram of the cathode readout paths and examples of the shape of the Buckeye amplifier signal.

Testing of the cathode strip electronics began with checking the CFEB-cathode strips connectivity. The intrinsic AFEB test pulse at maximum amplitude was used to generate a charge on the strips through wire-strip capacitor coupling. Dead channels and channels disconnected from the strips were easily detected.

The offsets (pedestals) of the strip readout channels and the noise of the SCA (rms of pedestals) were measured by randomly sampling the quiescent outputs of the amplifiers. A data analysis routine also found the dispersion of the 64 SCA means for each strip (full pile-up loop), and variation in the 8 consecutive readout time-bin values. Any cases of extra noise were investigated and about 2% of the boards were returned to the production site for repair.

The CFEB design allows the injection of a calibrated test pulse to the Buckeye chip channels through high precision capacitors (1%). This test pulse can be delayed relative to the trigger in 16 steps of 6.5 ns each to make a high precision scan of the time shape of the pulse of the Buckeye chip (Fig. 6). In this test the level and the time shape of the strip cross-talk, which are important for precise determination of the muon hit position, were also found. Another scan over the test pulse amplitude gives the calibration of the slope and intercept of the preamplifier output signal versus the DAC code of the input test-pulse, and quantifies the nonlinearity of the preamplifier response.

The test of the comparator readout path (Fig. 6) involves measurements of each comparator threshold, noise, and output signal timing. The comparator thresholds and noise levels were found by making a scan over the external threshold at 2 sequential test pulse amplitudes (15 and 40 fC). As in case of the AFEB, the sharpness of the comparator response turn-off curve characterizes the noise value. The DAC value at the 50% efficiency point of the comparator response defines the threshold corresponding to the injected charge. The parameters of a linear fit of the thresholds corresponding to 15 and 40 fC injected charge defined the slopes and offsets of comparator signals, which were also monitored.

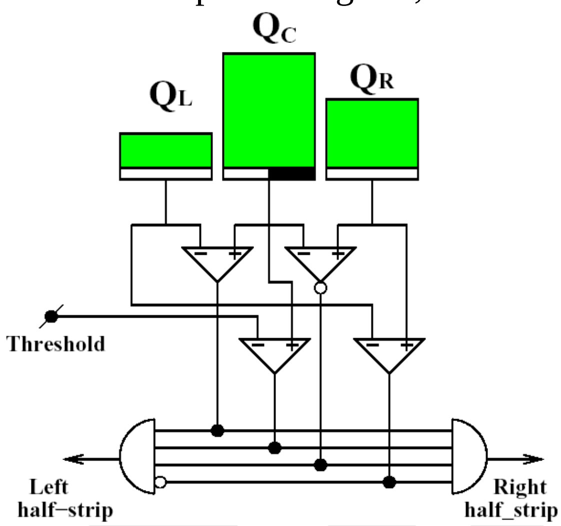

Fig. 7. Scheme of the strip comparator network.

The relative timing of comparator responses was checked by making a scan over the time delay with respect to the trigger of the 100-fC test pulse. Each comparator channel was characterized in terms of the time offset relative to the average time response of the CSC comparators. No deviation of more than 25 ns was accepted.

Finally, the right-left comparator logic (Fig. 7) was tested by pulsing 3 adjacent strips at the same time with amplitudes in the ratios 1:3:2 and 2:3:1. The CFEB design does not allow for direct measurement of the performance of the comparators, which carry out an analog comparison of voltages from neighbor strips. This was recovered in the data analysis of a long cosmic ray run.

The total percentage of replaced CFEBs, including single channel failures, was 9.3%, which is related to the complexity of the board and the large number of channels per board (96 analog and digital channels).

4.4 Tests with high voltage

4.4.1 Efficiency plateau

The performance validation tests were completed with a set of tests carried out with HV applied to the chamber. The CSC plateau efficiency for charged particle registration was measured based on the ALCT and the TMB trigger requirements for finding a stub with at least 4 hits in the chamber planes in a pattern consistent with a muon track coming from the interaction point. The measurements were taken at nominal AFEB and comparator thresholds of 20 fC. An example of measured count rates versus HV is shown in Fig. 8. The difference between the ALCT and TMB trigger count rates on the plateau is due to the difference in solid angle selection between the ALCT and the TMB trigger patterns. The CSC background noise was measured at HV=3600 V (at 3000 V for ME1/1 CSCs). The triggers were generated by the ALCT based on single wire group hits and by the TMB based on single comparator hits. In parallel with wire group count rates, the probabilities of isolated hits and after-pulsing were also monitored. In general, the CSC background noise level depended on the chamber size and environment where the measurements were taken. The typical noise level varied between 1 kHz for ME1/1 to 3.5 kHz for ME234/2 chambers. If extra noise was detected, the HV value on the sector in question was raised up to 3.8 kV and the sector was kept under this voltage for 24 h. If the noise level remained at its original value, then negative HV was applied to the sector and slowly raised to 3.3 kV. A limit on the training current was set to 50 µA. Usually, after training for 30 min at 3.3 kV the count rate dropped to an acceptable level.

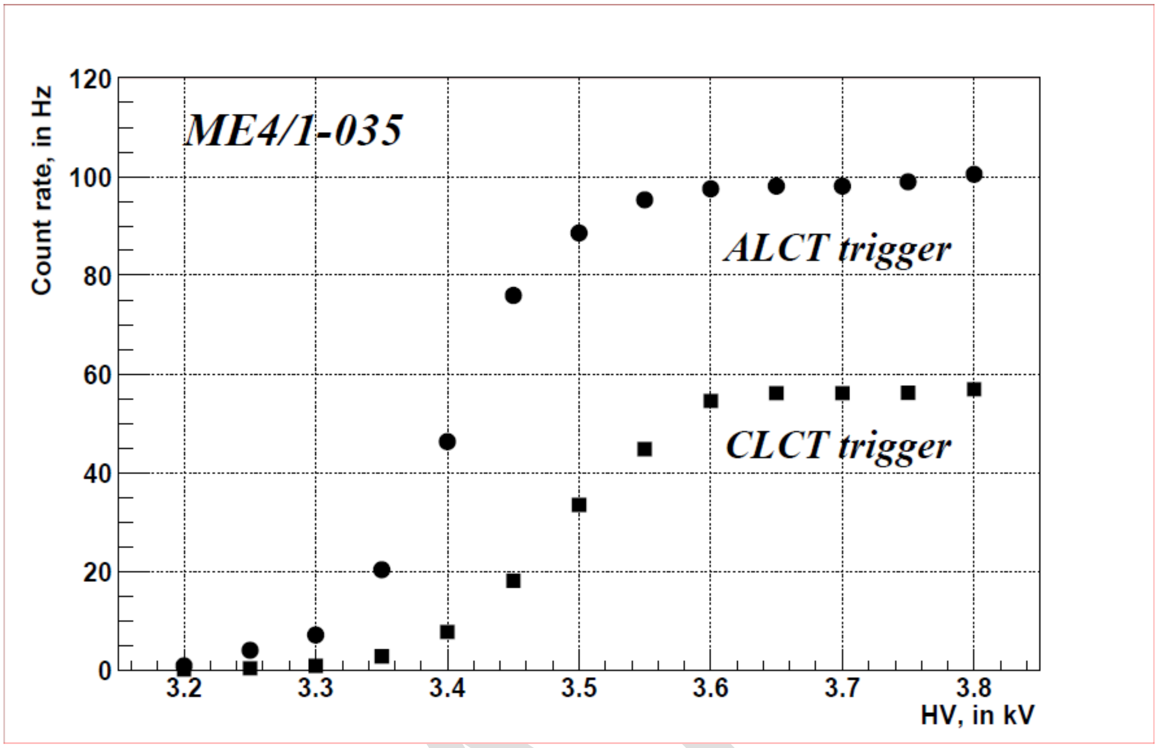

Fig. 8. The cosmic ray particle count rate for one of the ME4/1 chambers based on ALCT and TMB (CLCT) trigger decisions.

4.4.2 Trigger electronics performance tests

The capability of the ALCT to make trigger decisions in normal and high hit-rate environments was checked using cosmic-ray particles and a non-collimated 20-µCi Co^{60} gamma source. Different trigger conditions (1 hit in any plane of the CSC, 2 simultaneous hits in any 2 planes of the CSC that satisfied muon track "roads" through the 6 layers, etc., and finally tracks with 6 hits) were checked. The trigger signals were required to arrive at the ALCT within a time interval of 75 ns. Histograms of "key" wire group (a wire group in the 3rd plane from the interaction point most likely crossed by a trigger particle) occupancies in the presence of the radioactive source for 4 different trigger requirements are shown in Fig. 9. The count rates of the first 2 trigger settings were mainly caused by secondary electrons from gammas from the radioactive source, whereas cosmic ray particles were responsible for ALCT triggers with 3 or more simultaneous hits.

A similar test was performed to check the capability of the comparator network to provide adequate trigger information to the TMB. No ALCT or CFEB was rejected during these tests.

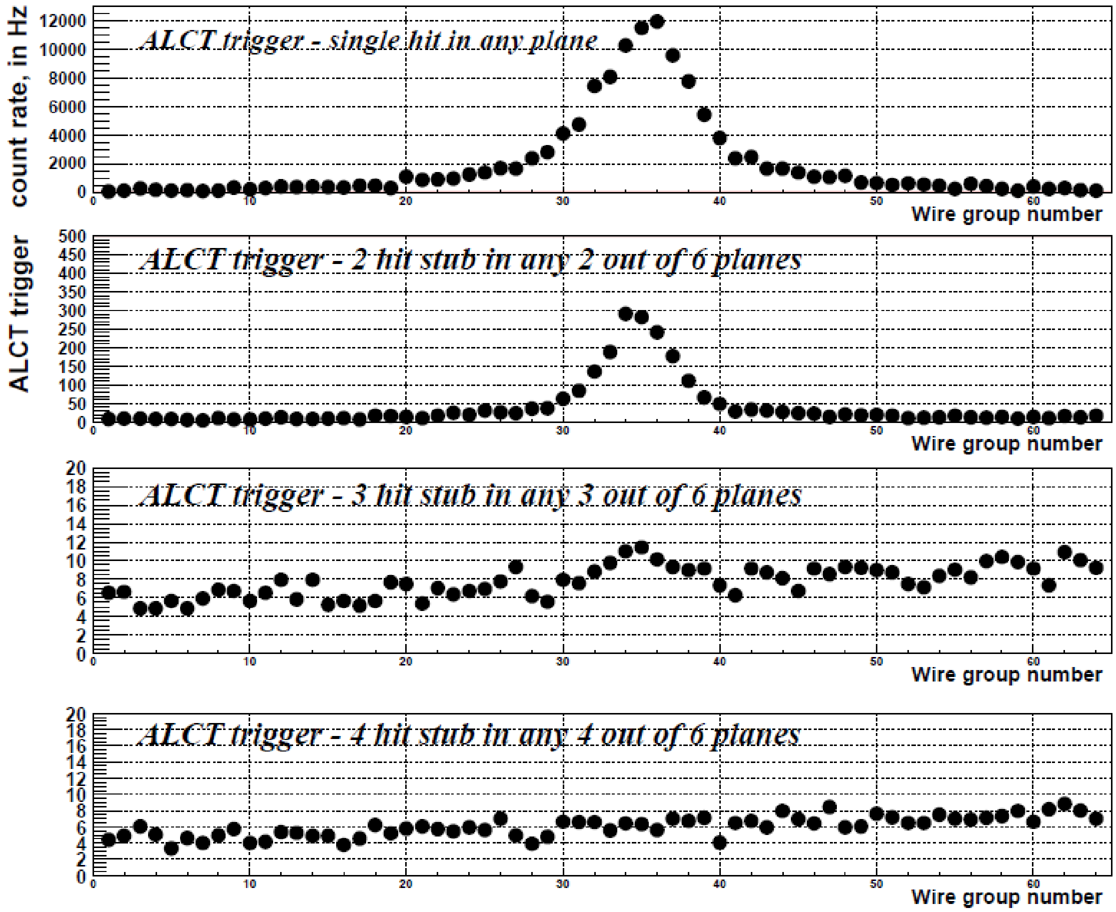

Fig. 9. “Key” wire group occupancies for different ALCT trigger conditions in the presence of the Co^{60} radioactive source.

4.4.3 High statistics cosmic-ray run

Many aspects of the chamber performance were measured in a long cosmic-ray run. One hundred thousand particles were detected by each chamber to determine the wire group, strip, and comparator track efficiencies, plane space resolutions, and chamber plane misalignment, and to verify the chamber time resolution. The absolute gas gain mapping of each plane and the functionality of the comparator network were also tested.

The data analysis algorithm is based on the reconstruction of a cosmic-ray track in the chamber. Track candidates with at least 5 hits were selected for the analysis. Signals from the plane under investigation were not used in the line fit of the cosmic-ray track. The quality of the observed tracks, like strip cluster efficiency, comparator track efficiency, and average comparator offset from track position were checked. The deviation of the strip cluster from a line, which is assumed to be the cosmic-ray track, was calculated to characterize the space resolution of the plane. The distribution of strip residuals along the chamber was used for finding plane misalignment. The results of relative position shifts of the planes inside a chamber showed that plane misalignment was within the specification range (~100 μm) and could be corrected offline.

The CSC space resolution is very sensitive to the strip signal-to-noise ratio. It constrains a certain limit on the CSC gas gain non-uniformity. To find the gas gain distribution within the CSC, each plane was divided into 15 (for most of the CSCs) or 25 segments (ME234/2). For each segment the accumulated spectrum of strip signals was fitted with a Landau distribution. The peak positions were used for CSC gas gain mapping. Corrections to the HV sectors to equalize the gas gain in each plane and to reach the necessary signal-to-noise ratio were calculated. An analytical fit of the gas gain dependence from the HV [4] was used. The corrections were stored in the CMS database.

Finally, the performance of the comparators, which define the particle hit position within half-strip accuracy (Fig. 7), was studied. For each strip, events in which particles crossed a plane in the vicinity of the strip were selected. Then the left and right half strip comparator efficiencies were analyzed as a function of signal amplitude difference between the left-right neighboring strips and between pairs of adjacent strips including the strip under investigation. The accumulated distributions were fitted with the **erf**-function. The parameters of the fit were used for the comparator offset and noise estimations. The limits for the offset and noise were set to 4 ADC counts (4 fC). No CFEBs was rejected because of noise or large offset.

5. Pre-installation Testing and Post-installation Commissioning

To uncover any damage that might have occurred during CSC transportation to CERN, each chamber had to pass the full FAST site testing procedure (except for the high statistic cosmic-ray run) in a storage area (ISR) upon its arrival. No major problems (e.g., broken wires, problems with HV connectivity, or unacceptable gas leaks) were found. Nevertheless, the tests at CERN revealed quite a few instances of minor mechanical damage like loose screws, unlocked connector latches, broken connector shells, and even loss of cable ground connections due to bad original soldering. Most of these faults caused some test to fail and were found by subsequent visual inspections. Unexpectedly, the tests at CERN discovered new kinds of CSC problems such as shorts between neighbor wire groups and wire groups disconnected from amplifier inputs. An analysis showed that problems during chamber assembly, such as overheated amplifier protection resistors, were the cause of dead channels. A few minor problems were also found on LVDBs. They were related to faults during board assembly, which caused gradual development of errors in reading the actual currents of the LV supply channels. The number of serious problems was substantially reduced relative to the FAST sites. For example, the number of replaced electronics boards was about 5 times less. Most of the problems encountered were fixed at the ISR. Chambers that successfully passed this stage of quality control were certified as operational and were prepared for installation on the steel disks.

Taking into account the time constraint for CSC installation, the number of tests for post-installation CSC commissioning and the event statistics of some tests were reduced. Only the most critical electronic tests were selected based on the FAST sites experience. The CSC gas leak rate was measured in the detector assembly building for groups of chambers connected in series, as they will be operated in CMS. No leak was detected because of CSC problems, but one chamber caused a factor of 6 reduction in the gas flow in one branch of 4 chambers. The chamber was removed from the disk and a piece of cleaning fabric blocking the gas flow was found and removed.

Then all installed chambers passed a broken wire test along with a 24-h HV test at 3.8 kV. No broken wire was found out of about 2.32 million wires. Only 2 chambers did not pass the HV “burn-in” test due to HV current trips and were replaced. A piece of wire in the sensitive volume of one CSC and a few low tension wires in another (local fault during production) were the reasons for the HV trips.

The test of functionality of the low voltage distribution system helped to find a few problems related to damage of low voltage cable connectors. It also helped to identify a few failures of LVDBs similar to the ones found at the ISR FAST site.

For the anode readout pathway, wire group connectivity and testing of the AFEB thresholds and analog noise were chosen for CSC commissioning. In all, 9 wire groups were disconnected from the amplifier inputs and 2 pairs of wire groups were short-circuited.

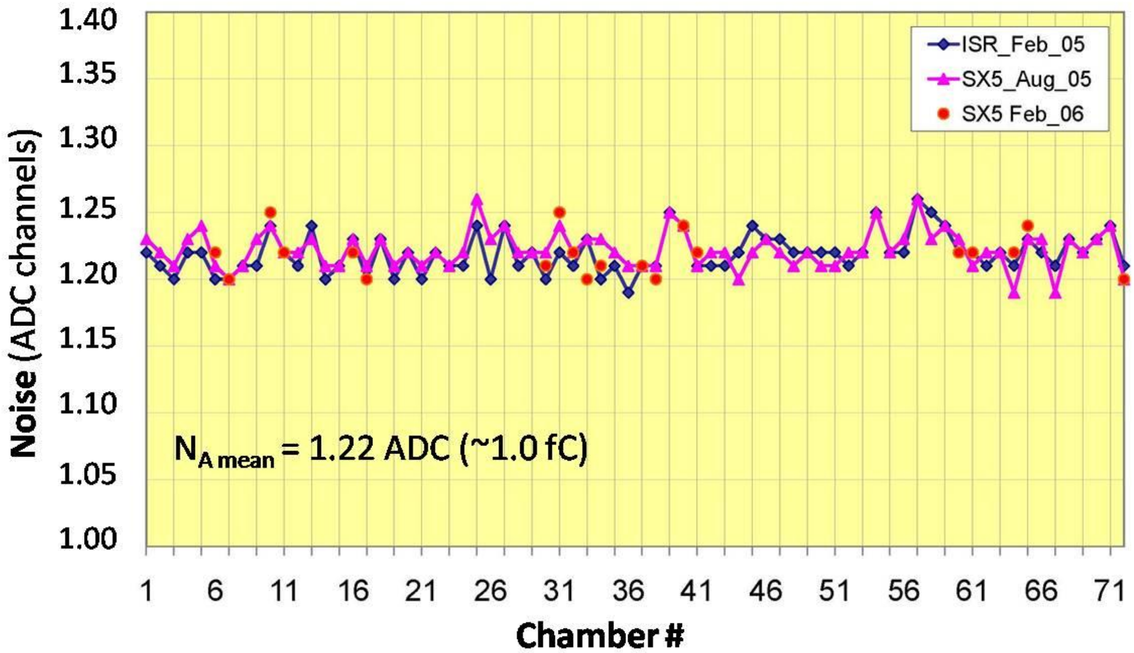

Fig. 10. Average AFEB analog noise of ME1/1 CSCs measured at the ISR FAST site at CERN (diamonds), after chamber installation on the disks (triangles), and 6 months later (circles).

Measurements of the average AFEB analog noise of the ME1/1 chambers (Fig. 10) were taken at the ISR FAST site at CERN, then after the chambers were installed on the steel disks, and then 6 months later. Figure 11 compares the AFEB noise levels for 6 types of CSCs measured at 3 different locations: at the FAST sites, at the ISR at CERN, and mounted on the steel disks. The AFEB noise level has not changed for any type of CSCs since the electronics was installed and it remains within the specification range of 1.2 fC. Figure 12 shows the difference in AFEB thresholds of all CSCs (except ME1/1) measured in the storage area at CERN, and after CSCs installation on disks is shown. No noticeable drift of the AFEB thresholds was observed.

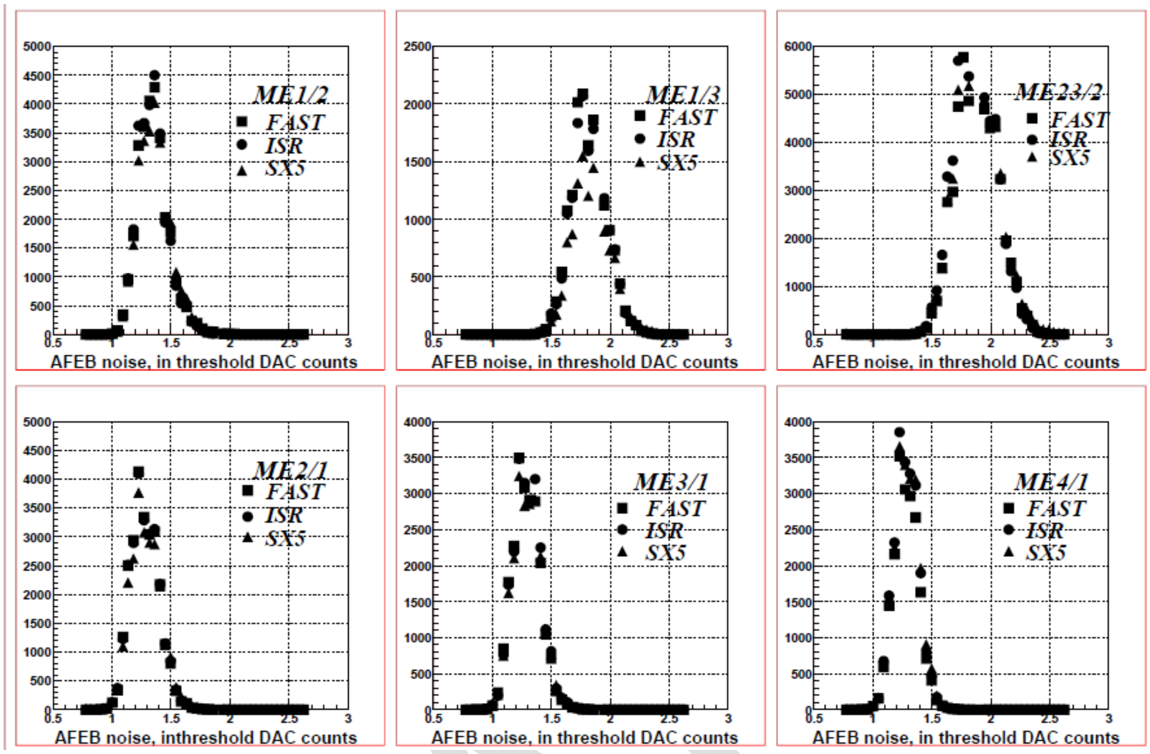

Fig. 11. Distributions of AFEB analog noise for all CSCs (except ME1/1) measured at 3 different locations: at the FAST sites, at the ISR at CERN, and in the CMS detector assembly building (SX5).

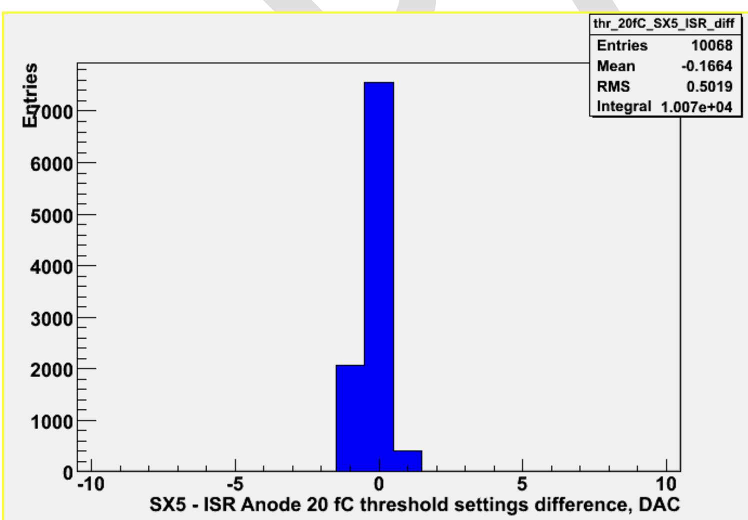

Fig. 12. The difference between AFEB thresholds of all CSCs (except ME1/1) measured at the ISR at CERN and during CSC commissioning in the detector assembly building.

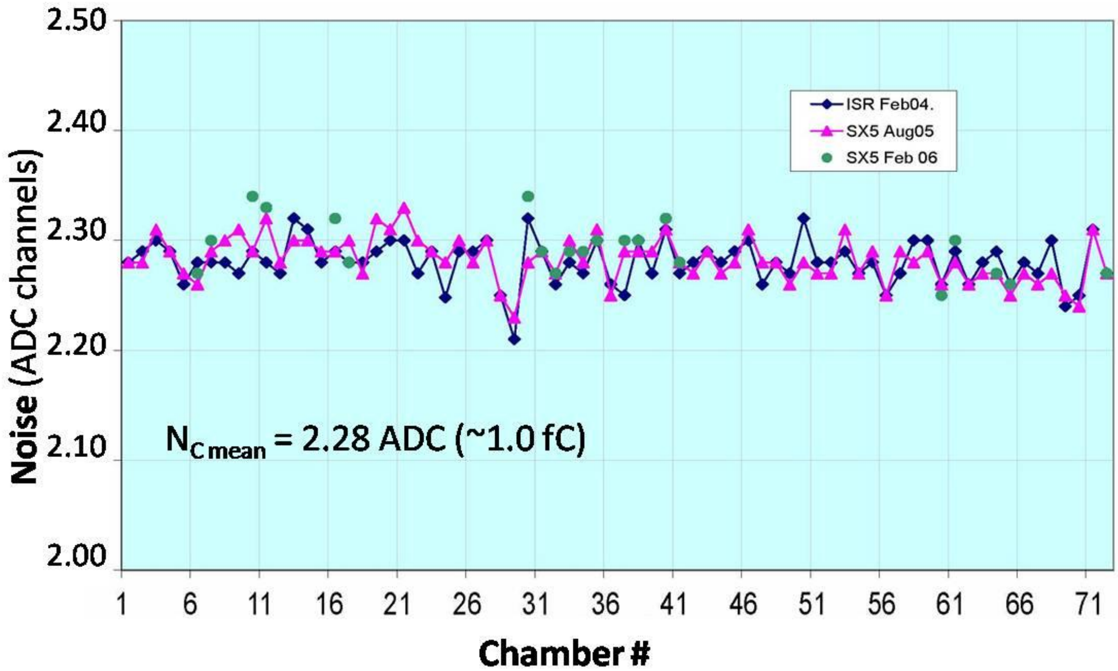

Fig. 13. Average RMS of SCA pedestals for ME1/1 chambers measured at the ISR at CERN, then after chambers installation on the CMS steel disks, and then 6 months later.

The strip connectivity, SCA noise, and comparator thresholds were checked for the cathode readout pathway. In Fig. 13, the average rms values of SCA pedestals are shown for ME1/1 as they were measured at the ISR at CERN, on the steel disks during CSC commissioning and 6 months later. In Table 1, the rms of SCA pedestals, the comparator thresholds and noise measured at 3 stages of quality control are shown for the 6 types of CSCs. The noise level of the SCA readout was within specifications (-1.5 fC). No drift of comparator thresholds has been seen since the electronics was put on the chambers. Only 0.6% of CFEBs were replaced during the CSC commissioning and subsequent CSC maintenance. These have been mainly due to the failure of individual channels or on-board ASIC chips.

The background noise of the wire groups and cosmic muon trigger rates at nominal HV were chosen as the main criteria for CSC commissioning with HV. Unexpectedly, about 5% of the installed chambers showed an increase in the noise level for some readout channels. We connected the observed local noise increase to the fact that once a chamber was produced it was stored, transported and tested in a horizontal position. Some leftover dust or debris inside the gas volume that had not been removed during the production could fall into the sensitive area when the chamber was placed vertically on a steel disk. Most of the noisy channels were eliminated by training the chambers in situ with either direct or reverse HV applied.

However, in the case of 2 chambers the training failed to suppress the local extra noise and the CSCs were replaced. The final distributions of wire group hit rates for 6 types of CSCs are shown in Fig. 14. The rates are mostly defined by terrestrial radioactivity and cosmic-ray background. The distributions have very small tails and there are only a few wire groups in the system with a noise level of a few tenths of Hz.

Table 1. Comparison of the strip readout performance measured at FAST sites, at the ISR at CERN, and on the steel disks.

CSC	rms of SCA pedestals in ADC counts			Comparator thresholds in DAC of thresholds			Comparator noise in DAC of thresholds		
	FAST	ISR	SX5	FAST	ISR	SX5	FAST	ISR	SX5
ME1/2	1.5±0.1	1.5±0.1	1.5±0.1	41±6	39±7	42±5	1.5±0.3	1.4±0.1	1.4±0.1
ME1/3	1.5±0.1	1.5±0.1	1.5±0.1	39±6	42±6	43±5	1.5±0.2	1.4±0.1	1.4±0.1
ME23/2	1.9±0.1	1.9±0.2	1.9±0.2	37±8	37±10	36±5	1.6±0.2	1.6±0.2	1.6±0.2
ME2/1	1.6±0.1	1.6±0.1	1.6±0.1	42±5	36±5	41±5	1.6±0.3	1.5±0.1	1.5±0.2
ME3/1	1.6±0.1	1.6±0.1	1.6±0.1	37±7	41±5	41±5	1.5±0.2	1.5±0.1	1.4±0.2
ME4/1	1.5±0.1	1.5±0.1	1.5±0.1	43±6	40±5	41±5	1.5±0.2	1.4±0.1	1.4±0.1

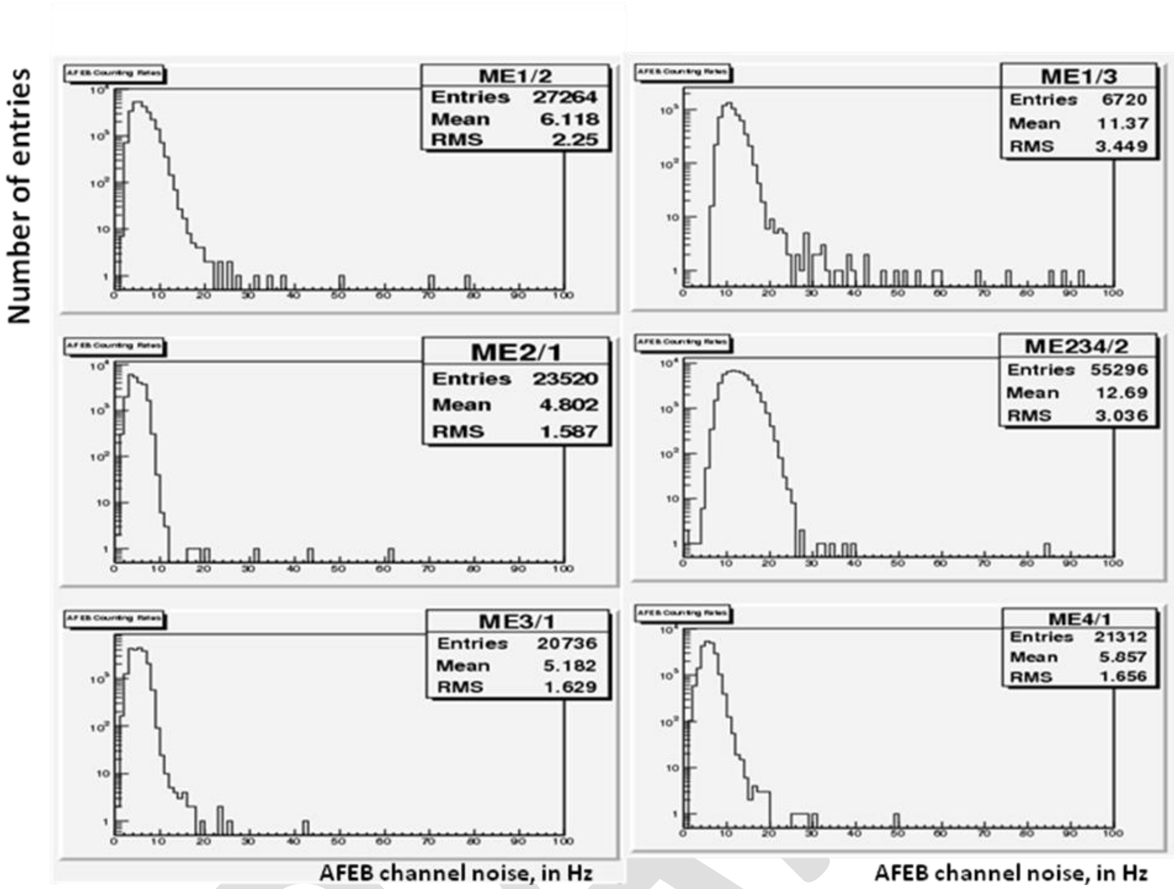

Fig. 14. Wire group count rates at nominal HV for different types of CSCs.

In Fig. 15, CSC cosmic muon trigger rates are shown as a function of the chamber angle position on a steel disk. The muon trigger rates of the CSCs were mainly defined by the sizes of the chambers and their positions on the disks. The observed sinusoidal-type dependence comes from changing the orientation of solid angles, in which the ALCT and the TMB (CLCT) select the cosmic muons. The 29º tilt of the ME1/1 anode wires relative to the wires of other chambers is also clearly seen.

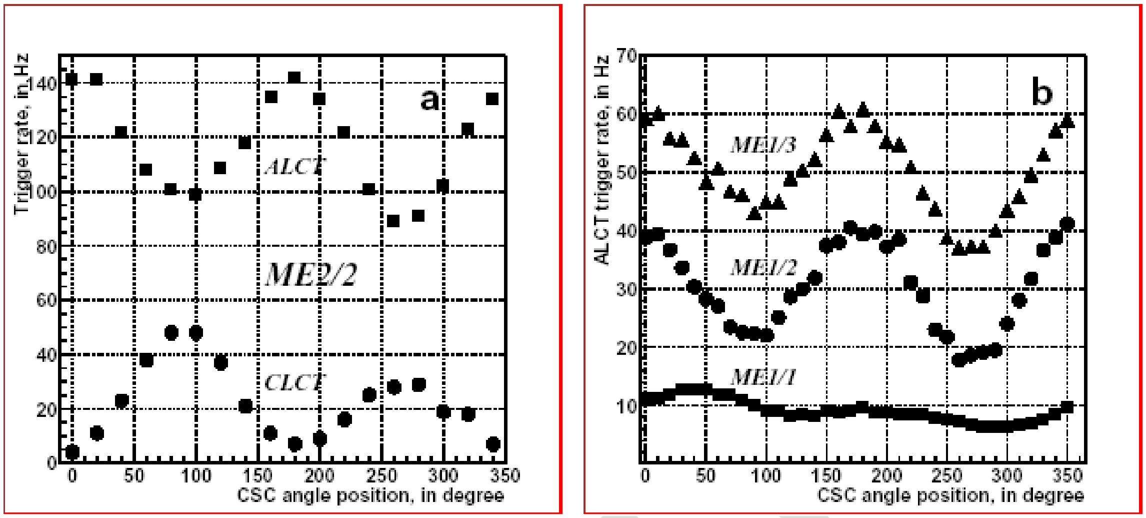

Fig. 15. CSC cosmic-muon trigger rates as a function of chamber angle position on the disks. a) ALCT and CLCT trigger rates for ME2/2; b) ALCT trigger rates for CSCs belonging to the first muon station.

6. Summary

The final installations of 468 CSCs on the steel disks of both endcaps of the CMS detector and their commissioning with the portable set-up have successfully been completed. The key to reaching this milestone was the careful program of quality assurance, which included comprehensive rechecking of CSC performance. The testing procedure and the sets of standard equipment distributed through the production sites allowed us to efficiently regulate the testing process. The common software and data analysis algorithms made possible the sharing of information about test results and the problems we encountered, and to enable the compilation of an extensive history of repeated tests for each CSC.

More than 500 CSCs (including spares) were produced, assembled with the on-chamber electronics and tested at the FAST Sites. During the first stage of quality control of the CSCs, problems were mostly single channel failures, which resulted in the replacement of about 10% of the front-end boards. Analysis of chamber performance showed that the main CSC parameters were within the required specifications.

The chambers were rechecked at the ISR FAST site at CERN before they were installed on the endcap disks. The number of detected problems was substantially reduced relative to the FAST site operations. Nevertheless, some new minor problems with the CSCs and on-chamber electronics were discovered and fixed.

Post-installation CSC commissioning confirmed that the system is gas tight and that there was not even a single broken wire out of 2.32 million wires. Only 5 CSCs were replaced because of HV current trips (2 chambers), unexpected high noise level in some local areas (another 2 chambers), and gas blockage in one chamber. About 0.25% of chamber HV segments were trained with reversed HV to eliminate local noise, which showed up only after the chambers had been installed on the steel disks. Less than 1% of the front-end boards were replaced at the final stage of the quality control procedure. Test results showed no change in on-chamber electronics performance. The measured anode and cathode noise levels (~1.2 fC for anode and ~1.5 fC for cathode) agreed closely with the noise level during post-assembly and pre-installation validation tests.

The CSCs have been prepared for the final commissioning with peripheral crate electronics and all support subsystems.

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