Summary of FAST Site Tests and Procedures

Brief Summary of FAST site test results

TESTS OF THEIR INDIVIDUAL RESULTS: PLOTS AND CALIBRATION TABLES			UNITS	LIMITS	
Test 1	*	**Broken Wires:** Check for broken wires after transportation (I at HV=1000 V)	µA	--	10
Test 2	*	**HV Connectivity:** Check for HV connectivity	µA	see specs	
Test 3	1	**Gas Leak:** Gas leaks on arrival	cc/min	--	1 or 2
Test 4	1	**Long-Term HV Test:** History of current during 2 months of long-term HV test	µA	see specs	
Test 5		**Relative Gas Gain Map (with radioactive source):**			
	1	Map of gas gain at 6x(HV segments) points per plane normalized on plane-average		--	--
	*	Check for absence of self-sustaining discharges after removing the radioactive source	µA	--	0.5
Step 6		**Assembly:**			
	*	Assemble chamber with cooling plates, electronic boards, cables, and misc. mechanics. Enter info in database	--	see specs	
Test 7	1	**Water Leak:** Check for cooling plate leaks	--	see specs	
Test 8	1	**Low Voltage:** Check in/out voltages and input currents on LVDB	Volts, Amps	see specs	
Test 9		**Slow Control Test:**			
	1	LVDB/LVMB: read out voltages/currents; check switching off/on of individual boards.	Volts, Amps	see specs	
	2	ALCT Self-Test (slow and fast control FPGAs);	misc.	see specs	
	3	Test strip pulse amplitudes	mV	???	???
Test 10	*	**HV-On Qualitative Test:** Check events on the event display (scintillator cosmic ray triggers)	--	see specs	
Test 11		**AFEB Counting Noise (at 3600 V and 3800 V):**			
	1	Noise counting rate at 3600 V	Hz	5	100
	2	Isolation probability at 3600 V (check for interconnected or strongly coupled wire groups within the same plane)	prob.	0.1	--
	3	After-pulsing probability at 3600 V	prob.	--	0.05
	5	Noise counting rate at 3800 V	Hz	5	100
	6	Isolation probability at 3800 V (check for interconnected or strongly coupled wire groups within the same plane)	prob.	0.1	--
	7	After-pulsing probability at 3800 V	prob.	--	0.05
Test 12		**AFEB connectivity:**			
	1	CSC-AFEB-ALCT connectivity and check for cable connection mix-ups (between planes only)	prob.	0.95	--
	2	Cross-talk probability between pair-planes sharing the same AFEBs: 1-2, 3-4, 5-6	prob.	--	0.05
	3	Cross-talks probability between non-pair-planes planes	prob.	--	0.01
Test 13		**AFEB Threshold and Analog Noise:**			
	1	AFEB analog noise (fC) at Qin=30 fC	DAC		
	2	DAC codes for 30-fC thresholds (per channel)	DAC		
	3	Table of chip-averaged 30-fC threshold DAC codes	DAC		
	4	Spread of channel threshold values around the 30-fC chip-average	DAC		
	5	AFEB analog noise (fC) at Qin=50 fC	DAC		
	6	DAC codes for 50-fC thresholds (per channel)	DAC		
	7	Table of chip-averaged 50-fC threshold DAC codes	DAC		
	8	Spread of channel threshold values around the 50-fC chip-average	DAC		
	9	*“DAC code per fC”* slopes for each channel	DAC/fC		
	10	Table of chip-averaged *“DAC code per fC”* slopes	DAC/fC		
	11	DAC codes for 20-fC thresholds (per channel)	DAC	0	
	12	Table of chip-averaged 20-fC threshold DAC codes	DAC	0	
	13	Spread of channel threshold values around the 20-fC chip-average	DAC		

TESTS OF THEIR INDIVIDUAL RESULTS: PLOTS AND CALIBRATION TABLES			**UNITS**	**LIMITS**	
Test 14		**ALCT-AFEB Time Delay:**			
	1	Quality of delay vs code linearity (chi2)	Chi2		
	2	Delay Slope (ns/code) per channel	ns/code		
	3	Delay CODE1 per channel to equalize delays for AFEB-test pulse	code		
	4	Table of Delay Slope (ns/code) averaged per chip	ns/code		
	5	Table of Delay CODE1 per chip to equalize delays for AFEB-test pulse	code		
	6	Spread of channel delays around the chip-average at Delay CODE1 setting	code		
	→	Table of Delay CODE2 per chip to equalize delays for muon hits	code		
	→	Delays in response for the test-strip pulses compared to the expected pulse propagation time (cable length check)	ns		
Test 15		**CFEB Pedestals and Noise:**			
	1	All-inclusive pedestals (disregarding offsets between different SCA cells and different time samples)	ADC	400	800
	2	All-inclusive CFEB noise	ADC	2	6
	3	Spread of pedestal offsets for different SCA cells	ADC	--	3
	4	Spread of pedestal offsets for different time samples	ADC	--	3
	5	Overnight drift of pedestals (measured as RMS of short-term pedestals)	ADC	--	1
Test 16		**CFEB Connectivity:**			
	1	CSC-CFEB connectivity and check for cable are mixed up (plane-to-plane only)	ADC		
Test 17		**CFEB Calibration:**			
	1	DAQ-path pulse time spread around CFEB-average	ns	-50	50
	2	DAQ-path pulse amplitude uniformity	ADC		
	3	DAQ-path pulse shape uniformity	--		
	4	Left-strip cross-talk	--		
	5	Right-strip cross-talk	--		
	6	Long-range cross-talk	--		
	8	Calibrate ADC-vs-Qin: slope	ADC/DAC		
	9	Calibrate ADC-vs-Qin: intercept	ADC		
	10	Calibration non-linearity	--		
Test 18		**Comparator Counting Noise (at 3600 and 3800 V):**			
	1	Noise counting rate at 3600 V	Hz		
	2	Noise counting rate at 3800 V	Hz		
Test 19		**Comparator Thresholds and Analog Noise in strip-signal-over-threshold channels:**			
	1	Table of CFEB-averaged 16-fC threshold DAC codes			
	2	Spread of channel threshold values around the 16-fC CFEB-average			
	3	Table of CFEB-averaged 40-fC threshold DAC codes			
	4	Spread of channel threshold values around the 40-fC CFEB-average			
	5	*“DAC code per fC”* slopes for each channel			
	6	Table of CFEB-averaged *“DAC code per fC”* slopes			
	7	Comparator analog noise at Qin=16 fC			
	8	Comparator DAC codes for 16-fC thresholds (per channel)			
	9	Comparator analog noise at Qin=40 fC			
	10	Comparator DAC codes for 40-fC thresholds (per channel)			
Test 20		**Comparator Output Timing:**			
	1	Spread of comparator output delays with respect to CFEB-averaged	ns	-25	25

TESTS OF THEIR INDIVIDUAL RESULTS: PLOTS AND CALIBRATION TABLES			**UNITS**	**LIMITS**	
Test 21		**Comparator Logic:**			
	1	Check correctness of comparator logic decisions by injecting preset calibration signal triplets	prob.	0.95	1.05
Test 23		**Comparator Offsets:**			
	1	Offsets for neighboring strip comparisons: S(n+1) – S(n)	DAC mV		
	2	Analog noise for neighboring strip comparisons: S(n+1) – S(n)	DAC mV		
	3	Offsets for left/right strip comparisons: S(n+1) – S(n-1)	DAC mV		
	4	Offsets for left/right strip comparisons: S(n+1) – S(n-1)	DAC mV		
	5	Half-strip occupancy for cosmic rays	counts	1	--
Test 24		**Absolute Gas Gain Map (with cosmic rays):**			
	1	Map of Landau charge peaks at (CFEBs)x(HV segments) points per plane	ADC	--	--
	2	ΔHV corrections for each HV segment to equalize gas gains	Volts	--	--
Test 25		**ALCT trigger:**			
	1	1/6-, 2/6-, 3/6-, 4/6-, 5/6, and 6/6-ALCT trigger rates vs wire group (cut on 4/6)	Hz		
	2	Average quality bit for k/6-ALCT triggers vs wire group	--	--	--
	3	1/6-, 2/6-, 3/6-, 4/6-, 5/6, and 6/6-ALCT trigger rates vs wire group with a high rate gamma-source (cut on 4/6)	Hz		
	4	Average quality bit for k/6-ALCT triggers vs wire group with a high rate gamma-source	--	--	--
Test 26		**CLCT trigger:**			
	1	1/6-, 2/6-, 3/6-, 4/6-, 5/6, and 6/6-CLCT trigger rates vs wire group (cut on 4/6)	Hz		
	2	1/6-, 2/6-, 3/6-, 4/6-, 5/6, and 6/6-CLCT trigger rates vs wire group with a high rate gamma-source (cut on 4/6)	Hz		
Test 27		**High Statistics Cosmic Ray Test**			
	1	Plane misalignment vs wire group number	--	--	--
	2	Table of plane misalignment parameters	--	--	--
	3	Long-range cross-talks per plane for each CFEB	--	???	???
Test 28		**Trigger plateau:**			
	1	4/6 ALCT rate vs HV	Hz vs Volts	???	???
	2	4/6 CLCT rates vs HV	Hz vs Volts	???	???
Test 30	**1**	**Gas Leak:** Measure gas leaks before shipping to CERN	cc/min	--	1 or 2

Format of Results

Each test results in

- Plots, which contain:
  - header
  - measured parameters reflecting chamber/electronics performance usually plotted vs. channel number for six planes
  - summary histogram for all channels/planes
- Numerical info files (result files), which contain[1]:
  - header
  - measured parameters reflecting chamber/electronics performance or calibration constants[2]
  - and lists of bad channels (with all parameters measured and tagged for the reasons why they are bad)

All plots and result files should contain the following HEADER:

- Test number: Test name
- Result file number: Brief result description
- Chamber type-number
- FAST Site; Who performed test; Date of the test completed; *Data file name; DAQ software version*[3]
- *Date of Analysis, Analysis software version*
- Status of the most recent test/analysis: OK or FAILED[4], Signature

```
Test 11:            AFEB Noise Test
Test_11_1.result:   Noise (fC) vs channel at HV=3600 V
ME234/2-034
Test performed:     15-Nov-2001  UC  Volkov    datafile_0103.dat   DAQ-1.50
Analysis done:      15-Nov-2001  Analysis-2.00
FAILED, -Ignatenko
```

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[1] Exclusions: Long term HV test data file (lots of numbers!)
[2] the entries may have arbitrary text comments added by hand (after a specific marker, e.g., #)
[3] *In cursive*: this information is entered only when applicable
[4] Status refers to the full test (not to a particular result/plot)

Chamber Arrival

Purpose: Record the arrival date and any relevant comments on condition of a chamber box at the time of delivery or a chamber after opening the box (broken hooks, damaged boxes, excessively wet boxes, damage during handling, etc.). Tracking of chambers begins (and never ends after that) with their arrival to FAST sites after the 24-hour HV test at the primary chamber assembly sites. This is applicable to all FAST Sites: UF, UC, PNPI, IHEP.

Method: Use the “CSC Tracking” database.

Test 1. Broken Wire

Purpose: To identify whether any wires are broken after transportation.

Method: Broken wires would tend to short to the cathode plane. A single wire short circuit will result in current: I = HV / (R1 + R2), where R1=1 MOhm and R2=5 MOhm (~17 µA at HV=1 kV). More shorts will lead to even larger current (note that even single broken wire would likely ground many nearby wire groups due to curling and snapping back after the break). At HV=1000 V, the current for the entire chamber is required to be less than 10 µA (one needs to wait at least 10 s to allow the initial charging current to decay). There is no need to use working gas mixture—the test will work equally well for a chamber filled with air.

Results:

`test_01_01.result`	`Just header`

Example:

```
Test 1:             Broken Wire
test_01_01.result:  Broken Wire
ME234/2-034
Tests performed: 15-Nov-2001  UC  Ignatenko
Analysis done:   15-Nov-2001
OK, -Ignatenko
```

Test 2. HV Connectivity

Purpose: Check for broken connections in HV distribution

Method: Ramp-up HV on an individual HV segment with a fixed rate (V/s) and observe the value of charging up current that should be ~C·(dV/dt), where C is the total capacitance of all wire groups and their blocking capacitors in the segment. See instructions.

Results:

test_02_01.result	Just header

Example:

```
Test 2:              HV connectivity
test_02_01.result:   HV connectivity
ME234/2-034
Tests performed: 15-Nov-2001  UC  Ignatenko     DAQ-1.50
Analysis done:   15-Nov-2001  Analysis-2.00
OK, -Ignatenko
```

Test 3. Gas Leak (on arrival)

Purpose: Detection of gas leaks

Method: Chamber is over-pressurized with gas to 3 inches of water column equivalent and the leak is evaluated based on the drop of the overpressure in 24 hours. Follow the note outlining the leak rate measurement procedure.

Results:

test_03_01.result	Result 1: List of results: Rate (cc/min), Overpressure at start (" H20), date, # brief com’t # Detailed comments, history of repairs (location, method of repairing, etc.)

Example:

```
Test 3:             Gas Leak Test (incoming)
test_03_01.result:  Gas leaks
ME234/2-034
Test performed:  15-Oct-2001  UC Ignatenko    DAQ-1.50
Analysis done:   15-Oct-2001  Analysis-2.00
OK, -Ignatenko

9.5    1.0   10-Oct-2001   # Leak around a bolt #3 on AFEB chamber side
1.2    3.0   15-Oct-2001

# 11-Oct-2001: leak around bolt 3 along AFEB chamber side is found
  13-Oct-2001: the bolt hole was filled with RTV
```

Test 4. Long-Term HV Test

Purpose: Check long-term stability of CSC operation (to weed out infant “mortality/sickness”).

Method: Keep CSCs under HV for 2-3 months: 2 weeks at HV = 3600 V (nominal operation point),
2 weeks at HV = 3700 V,
1 month at HV = 3800 V (this stage can be longer up to 2 month when time permits)
Constantly monitor the dark current with the computer-controlled HV monitor program. Follow instructions.

Results:

test_04_01.result	History: HV increases, over-currents (start-finish time and current), trips (time), # actions, faulty segments
test_04_02.result test_04_02.ps	Result 2: History file that can be used with HV monitor program Plot 2: Full history picture printed out from HV monitor program

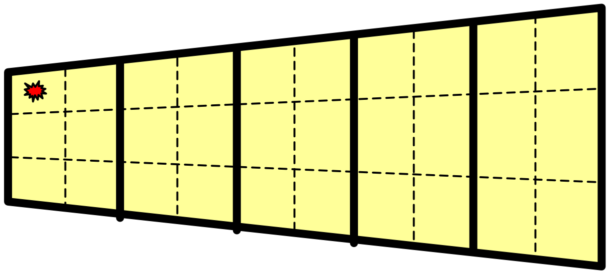
Examples:

```
Test 4:            Long-Term HV Test
test_04_01.result: History of HV and problems
ME234/2-053
Test started:    15-Feb-2002  UF Dolinsky
Test finished:   15-Apr-2002  UF Dolinsky
Analysis done:   15-Apr-2002  UF Dolinsky
OK, -Dolinsky

    02/15/02  11:20                3600 V
    03/01/02  12:16                3700 V
    03/20/02  14:21                3800 V
OC  03/21/02  19:41 - 19:46        3800 V      600 nA
OC  04/01/02  19:06 - 19:07        3800 V     1150 nA
    04/15/02  10:33                   0 V
```

Test 5. Relative Gas Gain Map (with radioactive source)

Purpose: A quick measurement of the gas gain uniformity. It also provides a cross-reference for absolute gas gains (and gas mixture quality) measured at different sites. In addition, one checks for self-sustaining discharges.



Method: A weak un-collimated source[5] is put over the chamber in the middle of grid cells as shown (6 cells per HV segment). The chamber is at 3600 V (Co-60) or 3800 V (Cs-137). The current is measured with a pico-ammeter from strips (all strips combined together). No cuts on the results are envisioned at this point. At the end of the test, after removing a radioactive source, one checks for any remaining self-sustaining discharges. HV segments with a self-sustained discharge exceeding 0.1 μA are to be recorded and trained.

Results:

test_05_01.result	6 Tables for each layer: Current/mCi (order as seen above)
test_05_01a.ps	Gas gain for each plane vs. wire grid cell no.
test_05_01b.ps	Cumulative histogram of gas gains normalized on average per plane

Example:

```
Test 5:             Gas Gain Test
test_05_01.result: Current (uA/uCi) vs (wire grid cell; strip cell) at HV=3800 V, Cs-137, 200 µCi
ME234/2-026
Test performed: 19-Nov-2001 UF Tavares
OK, -Tavares

Plane 1:
0.115  0.114   0.112   0.101  0.121   0.115   0.143   0.123   0.125   0.117
0.129  0.119   0.105   0.108  0.109   0.130   0.118   0.110   0.107   0.112
0.103  0.112   0.101   0.119  0.108   0.091   0.101   0.122   0.115   0.118

Plane 2:
0.063   0.070   0.081   0.073   0.096   0.080   0.095   0.069   0.069   0.084
0.049   0.079   0.088   0.091   0.087   0.117   0.103   0.089   0.111   0.092
0.061   0.068   0.085   0.077   0.089   0.075   0.072   0.076   0.080   0.068

Plane 3:
0.087   0.097   0.079   0.081   0.098   0.078   0.095   0.093   0.104   0.074
...
```

---

[5] Sc-137 or Co-60 100-200 μCi, not collimated.

Step 6. Assembly

Purpose: Assembly of a chamber with cooling plate, all on-chamber boards and cables, and all on-chamber hardware.

Method: Follow drawings and instructions specific for each step of assembly:

- Cooling plate
- AFEBs (and AFEB-CSC cables for ME1/2 and ME1/3)
- CFEBs
- CFEB cables
- ALCT
- ALCT-CSC cables
- ALCT-AFEB cables
- LVDB
- LVMB
- LVDB cables (do NOT connect them to CFEBs and ALCT before checking and recording voltage—see Test 7)
- CFEB, LVDB, and 2 ALCT covers.

Board numbers and their location on a chamber are to be entered in the FAST site inventory database. The database allows one to check the boards currently installed on the chamber.

Test 7. Water Leak

Purpose: Check for leaks around water inlet/outlet of the cooling plate once it is connected to the chiller.

Method: Hoses are connected to the water chiller system (chiller must operate at 4 atmosphere pressure). Check for leaks around both hose ends (immediately dripping water or accumulation of small water puddles within 24 hour time period).

Results:

test_07_01.result	pressure of water, # comments

Example:

```
Test 7:             Water Leak
Test_07_1.result:   Water Leak
ME234/2-034
Test performed:  15-Nov-2001  UC Ignatenko    DAQ-1.50
Analysis done:   15-Nov-2001  Analysis-2.00
OK, -Ignatenko

4.0
```

Test 8. Low Voltage

Purpose: Check LVDB power consumption and output voltages in unloaded and loaded conditions.

Method: First, before CFEBs and ALCT are connected to LVDB, record power consumed by the LVDB (power supply readings) and voltage at the *LV cable* output connector pins (use voltmeter). See documentation on LVDB pin assignment map and LV specifications.
Second, connect ALCT and CFEB boards, initialize them, and repeat the measurements.

Results:

test_08_01.result	2 Vin’s, 2 Iin’s, 4 ALCT Vout’s, 3 CFEB Vout’s for all CFEBs (LVDB unloaded) 2 Vin’s, 2 Iin’s, 4 ALCT Vout’s, 3 CFEB Vout’s for all CFEBs (LVDB loaded)

Examples:

```
Test 8:             Low Voltage
test_08_01_result:  2 input Vs; 2 input Is; 19 output Vs; #LVDB not loaded
                    2 input Vs; 2 input Is; 19 output Vs; #LVDB loaded and after CFEB, ALCT initialization
ME234/2-034
Test performed:  15-Nov-2001  UC Ignatenko
Analysis done:   15-Nov-2001
OK, -Ignatenko

LVDB not loaded:

Input Vs:           xxx   xxx
Input Is:           xxx   xxx

Output Vs:    ALCT  xxx   xxx   xxx   xxx
              CFEB1 xxx   xxx   xxx
              CFEB2 xxx   xxx   xxx
              CFEB3 xxx   xxx   xxx
              CFEB4 xxx   xxx   xxx
              CFEB5 xxx   xxx   xxx

LVDB loaded:

Input Vs:           xxx   xxx
Input Is:           xxx   xxx

Output Vs:    ALCT  xxx   xxx   xxx   xxx
              CFEB1 xxx   xxx   xxx
              CFEB2 xxx   xxx   xxx
              CFEB3 xxx   xxx   xxx
              CFEB4 xxx   xxx   xxx
              CFEB5 xxx   xxx   xxx
```

Test 9. Slow Control

Purpose: Perform self-tests of boards and their slow control functions.

Method:
1) LVDB-LVMB slow control functions and parameters to be readout.
   * Call a standalone LVMB-test program that performs the following checks:
     - Measure via DMB Vin, Vout, Iout for all LV inputs and outputs
     - Switch off/on individual boards via DMB and check all Vout, Iout (turned off channels should be zero, while others must remain within specs)
     - Repeat the cycle 10 times

2) ALCT SLOW and FAST control self-tests:
   * Measure with an oscilloscope test strip signal amplitudes at particular DAC setting (TBD)
   * Call an ALCT SLOW[6] and FAST[7] self-test sub-programs and verify that the returned codes are OK

3) CFEB slow control self-tests (TBD)

Results:

`test_9_01.result`	`LVMB: 19 currents and 21 Voltages with all boards powered`
`test_9_02.result`	`Test strip signal in mV at nominal DAC (6 values)`
`test_9_03.result`	`SLOW control firmware version, 4 ALCT voltages, 4 ALCT currents, ALCT Temperature` `FAST control firmware version`
`test_9_04.result`	`CFEB firmware version, CFEB1, CFEB2, CFEB3, CFEB4, (CFEB5) temperatures`

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[6] SLOW control self-test checks: firmware version, voltages, currents, temperatures, thresholds (ADC vs set DAC)

[7] FAST control self-test checks: firmware version, found vs generated pattern for a scan of patterns across all key wire groups

Test 10. HV-on Qualitative

Purpose: Before proceeding with detailed and sometimes time-consuming tests, check during 5-10 minutes cosmic ray events on the event display and using cosmic ray scintillator trigger. This is a qualitative test with no specific instructions.

Method: Use cosmic ray trigger and fully-expanded event display. Here are a few suggestions as for what one may want to look for:
- persistent hits on wire groups and/or excessive noise on strips
- missing planes
- timing of cathode signals on SCA displays

Test 11. AFEB Counting Noise

Purpose: Look for noisy wire groups. Also, look for short circuits (or significant cross-talks between wire groups) and chamber after-pulsing probability.

Method: Trigger on any AFEB hits (ALCT single-plane self-trigger mode). Count all wire groups with at least one hit anywhere within ALCT time window (range 16). Measured rates are to be as expected for each wire group. Look for short circuits or highly-coupled wire groups by measuring the probability of getting exactly one hit. Note that rates are to be corrected for DAQ readout dead time by measuring the actual ALCT rate with a free-running CAMAC scaler. The test is done at nominal and increased high voltages: 3600 V and 3800 V. AFEB thresholds (DAC values) are set to Q_threshold~20 fC using CMU calibration data.

Analysis details: An occupancy histogram is filled with one entry per hit for each wire group number with a hit. To calculate the rate, the number of entries n(wire#) is divided by the total time T of taking data and corrected for DAQ dead time by multiplying by a factor N_CAMAC_events/N_DAQ_events:

Rate(wire #) = n(wire#) / T * (N_CAMAC_events / N_DAQ_events)

→ change analysis: remove normalization per m

An isolated hits histogram is filled with one entry for each event that has only one hit anywhere in the chamber. Its purpose is to check for significant cross-talk: if two wires are coupled, their occupancies in the isolated hits histogram will be reduced. Probability is calculated as:

Isolation_probability(wire #) = n_isolated(wire#) / n(wire #)

After-pulsing probability: If there are more than one cluster of contiguous ALCT bins within ALCT time window (range 16) the event is considered to have after-pulses.

After-pulse probability(wire #) = n_with_afterpulses(wire#) / n(wire #)

Available histograms include:

hid = 2000	number of layers hit per event	
hid = 2000 + layer	wire occupancy vs wiregroup	
hid = 2000 + 10 + layer	isolated hit occupancy vs wiregroup	
hid = 3000 + 100 * layer + wg	wire hit times (range 1-32)	<--- will not work for ME2/1

Results:

test_11_01.result test_11_01.ps	Rate in Hz wire group vs. (plane, channel) at HV=3600 V
test_11_02.result test_11_02.ps	Probability of giving an isolated hit vs. (plane, channel) at HV=3600 V
test_11_03.result test_11_03.ps	Probability of after-pulsing vs. (plane, channel) at HV=3600 V
test_11_04.bad	Bad channels: (plane, wire#) R1 R2 R3 problem_code #comment
test_11_05.result test_11_05.ps	Rate in Hz per wire group vs. (plane, channel) at HV=3800 V
test_11_06.result test_11_06.ps	Probability of giving an isolated hit vs. (plane, channel) at HV=3800 V
test_11_07.result test_11_07.ps	Probability of after-pulsing vs. (plane, channel) at HV=3800 V
test_11_08.bad	Bad channels: (plane, wire#) R5 R6 R7 problem_code #comment

Examples:

```
Test 11:            AFEB Count Noise
test_11_1.result:   Rate in Hz vs (plane, channel) at HV=3600 V (threshold ~20 fC)
ME234/2-034
Test performed:  15-Nov-2001  UC Ignatenko    DAQ-1.50
Analysis done:   15-Nov-2001  Analysis-2.00
FAILED, -Ignatenko

      1      2      3      4      5      6
1   0.0    1.8  342.9    1.9    1.4    1.2
2   1.7    1.5    1.9    1.7    1.0    1.1
3   ...
...
64
```

```
Test 11:         AFEB Count Noise
test_11_5.bad:   List of bad channels: (plane, channel), Noise, Isolation, After-pulsing at HV=3600 V,  #comment
ME234/2-034
Test performed:  15-Nov-2001  UC Ignatenko    DAQ-1.50
Analysis done:   15-Nov-2001  Analysis-2.00
FAILED, -Ignatenko

(1,1)      0.0         F      0.0     F    Low Noise        # dead AFEB channel
(3,1)    342.9      1.00    367.2     F    High Noise       # noisy AFEB cannel
(2,3)      1.2      0.00      1.4  0.00    Low Isolation    # connected in Chamber to (2,4)
(2,4)      1.2      0.00      1.4  0.00    Low Isolation    # connected in Chamber to (2,3)
```

Test 12. AFEB Connectivity

Purpose: To check that AFEBs are all alive and connected to the wires. Also, check for absence of plane-to-plane cross-talks (note that plane pairs 1&2, 3&4, 5&6 share AFEB chips and may be prong to have cross-talk). Cable connections mixed between planes will be easily identified.

Method: One uses the ALCT test pulse generator (triggered by an external test pulse) to apply test pulses to the test strips of each layer in turn. The test pulse amplitude for ME23/2 chambers is fixed at Test Signal Code = XXX, V_test_pulse~XXX mV, which gives Q_in[8]~60 fC. For smaller chambers, the signal amplitude is yet to be defined. Signals should be seen on all wire groups of one layer. For all wire groups, check for cross-talk in paired planes (e.g, probability of signals in layer 1 when layer 2 is pulsed, probability of signals in layer 2 when layer 1 is pulsed, probability of signals in layer 3 when layer 4 is pulsed, etc.) and non-pair planes (e.g., probability of signals in layer 1 when layers 3, 4, 5, or 6 are pulsed).

Analysis details: An occupancy histogram is filled with one entry per event for each wire that has one or more hits (multiple hits within the ALCT time window count as one entry). Actually, one of three occupancy histograms is filled, depending on whether the hit wire is in the layer with the pulsed strip, its pair layer, or one of the other four layers.

Available histograms:

hid = layer	pulsed layer: number of hits vs wiregroup
hid = 10 + layer	"pair" layer: number of hits vs wiregroup
hid = 20 + layer	other layers: number of hits vs wiregroup

Results:

test_12_01.result test_12_01.ps	Efficiency vs. (plane, channel)
test_12_02.result test_12_02.ps	Cross-talk probability from pair-plane vs. (plane, channel)
test_12_03.result test_12_03.ps	Cross-talk probability from non-pair-plane vs. (plane, channel)
test_12_04.bad	Bad channels: (plane, wire#) R1 R2 R3 problem_code #comment

Examples:

```
Test 12: AFEB Connectivity Test
test_12_4.bad: List of bad channels: eff, pair-plane cross-talk, non-pair-plane cross-talk, problem code, #comment
ME234/2-034
Test performed:  15-Nov-2001  UC Ignatenko    DAQ-1.50
Analysis done:   15-Nov-2001  Analysis-2.00
FAILED, -Ignatenko

(1, 1)  0.01   0.000  0.000  Dead                             # chamber problem
(3,17)  1.00   0.023  0.000  High pair-plane cross-talk
(6,64)  1.00   0.005  0.002  High non-pair-plane cross-talk
```

---

[8] Q_in will be dependent on wire group width: Q_in = V_test_strip * C_test_strip_to_wire_group, where C_test_strip_to_wire_group=0.4 pF for ME23/2. In addition signal gets attenuated as it propagates along the test strip. So this setting should be sufficiently high to ensure that signals are reliably above threshold.

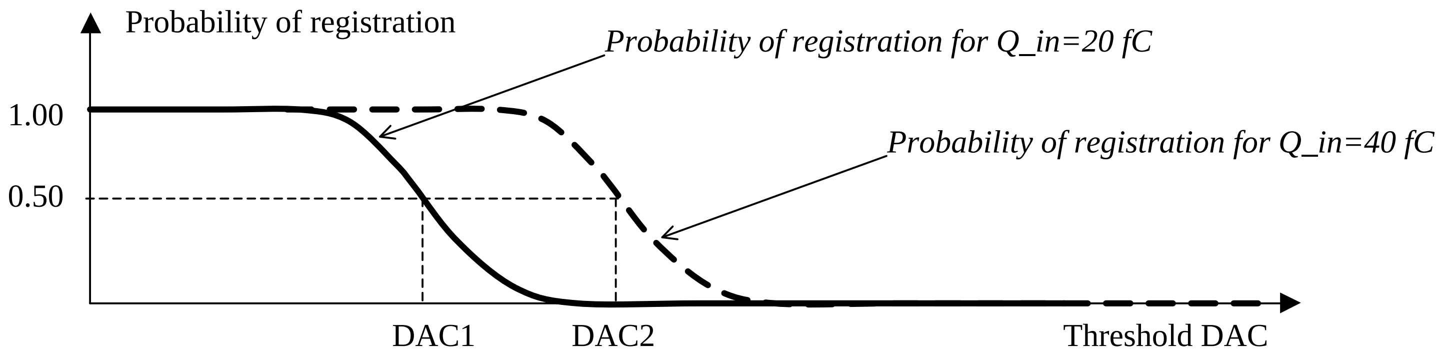
Test 13. AFEB Thresholds and Analog Noise

Purpose: To measure the threshold and noise of each wire group (using ALCT test pulse generator).

Method: One uses the ALCT test pulse generator (triggered by an external test pulse) to apply AFEB test pulses to all wire groups simultaneously. The test pulse amplitude is set at XXX DAC code, which gives V_test_pulse[9]~XXX mV, Q_in[10]~30 fC. The threshold is scanned from 0 to 79 in steps of 1 DAC count. Turn-off curve (efficiency vs DAC) is fit with an error function for the DAC value for 30 fC threshold (50% efficiency point) and AFEB thermal noise in DAC units (fit sigma)[11]. The best DAC30 value (average, excluding outliers) is picked for each chip. The scatter of channel threshold offsets (in fC) within a chip is checked.

The procedure is repeated for pulse amplitude set at XXX (DAC code for 50 fC) to yield two tables of DAC50 values (per channel and per chip) corresponding to 50 fC threshold.

Combination of both results gives DAC-vs-threshold slopes and 20 fC thresholds per channel and per chip.



Analysis details: A histogram of the number of events with a hit vs. threshold is filled for each wire group. There is no particular requirement on the hit time, only that it be within the readout window of 16 clocks (16*25=400 ns). Each histogram is then differentiated, the mean(i) of the new histogram is the threshold corresponding to 50% efficient DAC(i) and the rms(i) is the AFEB analog noise measured in threshold DAC units. Failure to find mean and/or rms is flagged with error code –1. For each chip, an average of DAC(i) values is taken, after excluding bad channels. The spread of DAC(i) values around DAC(chip) is checked. Analysis is done for test signal setting corresponding to 30 and 50 fC.

Slope is measured as (DAC50 – DAC30)/(50 fC - 30 fC). Channels tagged as bad in either 30 fC or 50 fC test signal runs will have slope set to –1 (no calculations of slope are performed). The 20 fC threshold codes, DAC20, are calculated as DAC20 = DAC30 – (slope)*(10 fC) and required to be settable, i.e. positive.

Available histograms:

hid = 4000 + 100 * layer + wire num events with a hit vs test pulse amplitude (30 fC run)
hid = 5000 + 100 * layer + wire num events with a hit vs test pulse amplitude (50 fC run)

---

[9] Can be probed at the AFEB connector
[10] Q_in = V_test_pulse * C_inner, where C_inner=0.24 pF is a built-in capacitance in AFEB chips.
[11] Due to occasional fit instabilities, this procedure is replaced by measuring mean and RMS of the histogram obtained by differentiating the turn-off histogram.

Results:

test_13_01.result test_13_01.ps	Noise(i) in DAC at threshold=30 fC vs (plane, wire#)
test_13_02.result test_13_02.ps	DAC30(i) for threshold=30 fC vs (plane, wire#)
test_13_03.result	DAC30(chip) for threshold=30 fC vs. chip#
test_13_04.result test_13_04.ps	Threshold offsets DAC30(i)-DAC30(chip) vs. (plane, wire#))
test_13_05.result test_13_05.ps	Noise(i) in DAC at threshold=50 fC vs (plane, wire#)
test_13_06.result test_13_06.ps	DAC50(i) for threshold=50 fC vs. (plane, wire#)
test_13_07.result	DAC50(chip) for threshold=50 fC vs. chip#
test_13_08.result test_13_08.ps	Threshold offsets DAC50(i)-DAC50(chip) vs. (plane, wire#))
test_13_09.result test_13_09.ps	Threshold slopes(i) in DAC/fC vs. (plane, wire#)
test_13_10.result	Threshold slopes(chip) in DAC/fC vs. chip#
test_13_11.result test_13_11.ps	DAC20(i) for threshold=20 fC vs (plane, wire#)
test_13_12.result	DAC20(chip) for threshold=20 fC vs. chip#
test_13_13.result test_13_13.ps	Threshold offsets DAC20(i)-DAC20(chip) vs. (plane, wire#))
test_13_14.bad	Bad channels: (plane, wire#) R1 R2 R4 R5 R6 R8 R9 R10 R11 R12 R13 problem_code

Examples:

```
Test 13: AFEB Threshold and Analog Noise Test
test_13_03.result: Optimal DAC1 values (hex code) per chip for 20 fC threshold
ME234/2-034
Test performed:  15-Nov-2001  UC Ignatenko    DAQ-1.50
Analysis done:   15-Nov-2001  Analysis-2.00
FAILED, -Ignatenko

AFEBs
 1  xxx    2  xxx    3  xxx
 4  xxx    5  xxx    6  xxx
 7  xxx    8  xxx    9  xxx
10  xxx   11  xxx   12  xxx
13  xxx   14  xxx   15  xxx
16  xxx   17  xxx   18  xxx
19  xxx   20  xxx   21  xxx
22  xxx   23  xxx   24  xxx
```

Test 14. AFEB-ALCT Time Delays

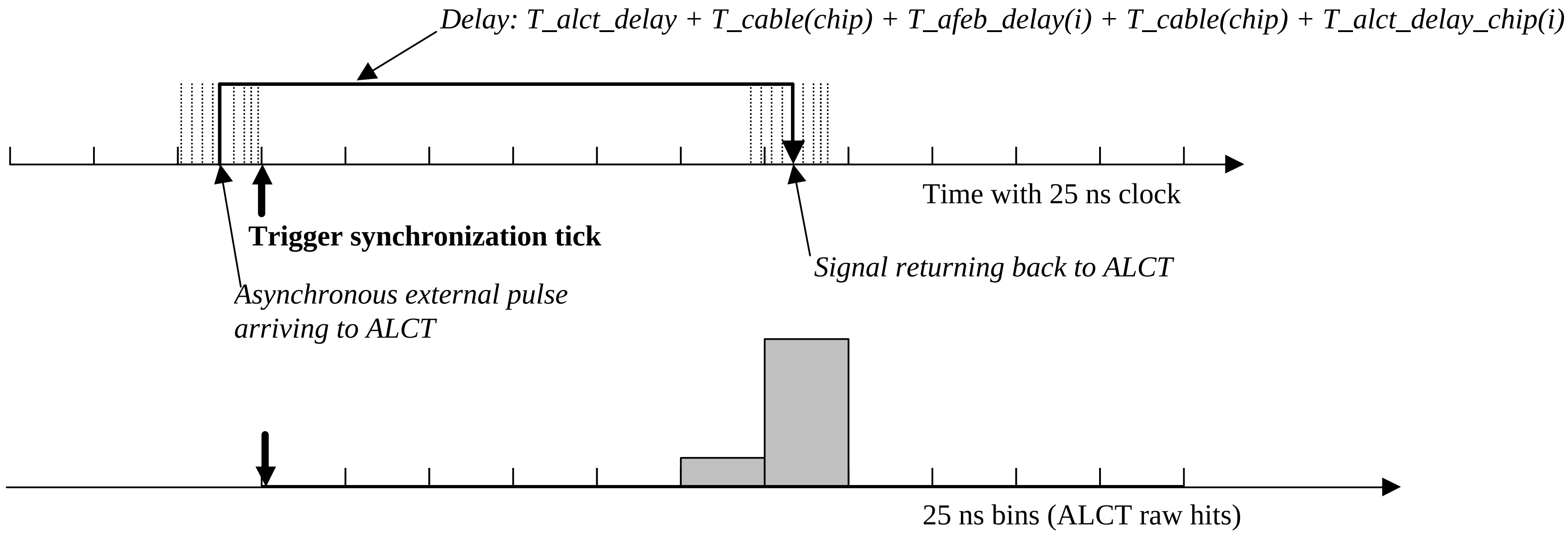
Purpose: Measure the constants needed to equalize the arrival times at the ALCT of the anode raw hits. (Equalization can only be done chip-by-chip.) This will remove delay spread in AFEB boards themselves and variations due to differences in AFEB-ALCT cable lengths. Also, verify that there are no mixups in AFEB-ALCT interconnections and that all cables are of the correct length.

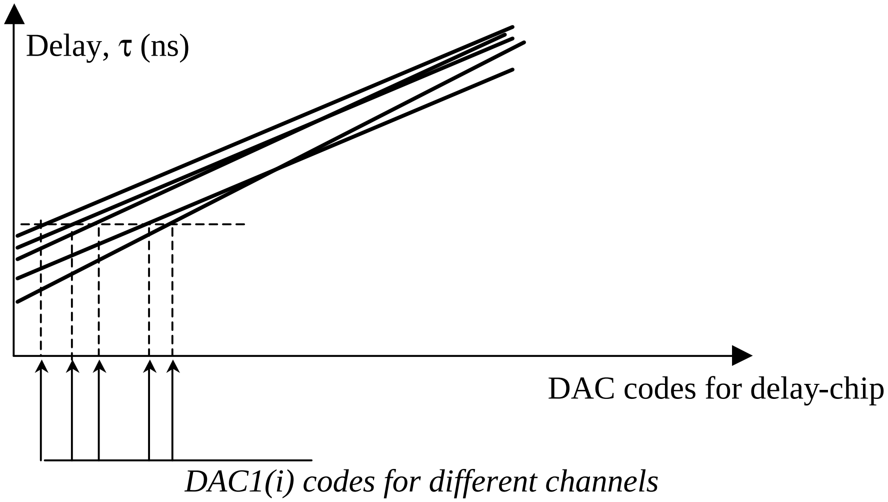
Method: Send external asynchronous (with respect to the 40 MHz clock) test pulses to ALCT to generate test pulses to all AFEBs (??? Code—-it must be large to ensure no threshold dependence). AFEB thresholds are set to ~20 fC. Signal will come back to ALCT at time T(i):

T(i) = T_external + T_alct_delay + T_cable(i) + T_afeb_delay(i) + T_cable(i) + T_alct_delay_chip(i)

The ALCT is set up to generate an ALCT trigger on arrival of the external pulse. The ALCT trigger T_alct_trigger will be synchronized by the 40 MHz clock. Therefore, there will be natural 25 ns jitter in the delay ΔT(i) between signal coming back to ALCT T(i) and the trigger T_alct_trigger.

Read back the discriminator hits. For each channel, the ALCT should have all hits latched in two adjacent bins. Define delay time as the weighted average of the two bins: τ(i) = (25 ns) * ((τ1*(%) + τ2*(%)). Ramp over delay code DAC settings (settings 0 - 15, or approximately 0 - 30 ns) and “plot” τ(i) vs. DAC.





Do a linear fit to delay vs delay code setting DAC. The fit gives slopes for delay chips (ns/DAC). Find average slope per chip: slope(chip). Do not use outliers in averaging. Then, find DAC1(i) values that equalize all τ(i) per channel. Get average DAC1(chip) per chip (outliers excluded).

Check for spread of remaining delay offsets: δτ(i) = (DAC1(i)-DAC1(chip)) * slope(i).

At last, convert DAC1(chip) values to DAC2(chip) values that should equalize arrival of muon signals:
DAC2(chip) = DAC1(chip) + T_cable(chip)/slope(chip).

Note that this test does not actually verify that ALCT-AFEB cables are actually of the correct length. Although cable mix-ups are not likely (the cables are clearly marked on both ends and come in one-chamber kits), they are still conceivable. To check that installed cables have correct destination (chamber length-wise[12]) and correct length, we conduct the following sub-test. Asynchronous pulses are now sent to tests strips (all planes simultaneously). The pulse amplitude code is the largest FF (hex code). Measure τ(i) same way as above. The farther away the wire group from the test strip input the longer it will take to respond due to propagation time along a strip (about 5 ns/m) and signal front deterioration as it runs along a test strip. Compare measured delays to predicted delays that are to be established after measuring the first few chambers.

---

[12] Mix-ups between different planes are easily identified in the AFEB connectivity test, Test 12.

Analysis details:

The data consists of a ramp over all possible delay settings (0 to 15, or approximately 0 to 30 ns). At each setting 2000 asynchronous test pulses are sent to all the AFEBs and the ALCT hits are read back. A time bin occupancy (leading edge of all hits) histogram is filled for each channel. For a particular delay setting and channel, the hits should all be in two adjacent time bins (two because of the jitter of the test pulse relative to the 40 MHz ALCT readout clock). The measured delay is taken to be the weighted average of the two bins (the largest bin and its largest neighbor).

After the measured delay is calculated for each delay setting, a linear fit to delay vs delay code is done for each channel. Average of slope(i) for all channels in a chip is calculated: slope(chip). Excluded outliers (bad channels) are those with chisq >100 and slopes falling out of range. Chips with no channels passing the limit tests are flagged with a delay setting of -1. DAC1(i) are calculated to equalize $\tau(i)$ to the good channel with the largest delay at DAC code=0. This will insure that all DAC1(i) values are positive. Average of DAC(i) values for all channels (excluding outliers) in a chip is calculated: DAC1(chip). DAC1(chip) settings will equalize delays for the AFEB test pulses.

The next step is to calculate delay code settings for muons:

DAC2(chip) = DAC1(cip) + T_cable(chip)/slope(chip)

The following is a table of delays (ns) in cables as measured with oscilloscope (each column corresponds to a tower of three AFEBs):

CSC type	1	2	3	4	5	6	7	8	9	10	11	12	13	14
ME234/2	18.0	18.0	15.0	15.0	10.0	10.0	6.8	6.8						
ME1/2	8.4	8.4	6.8	6.8	5.1	5.1	5.1	6.8						
ME1/3	10.0	6.8	5.1	5.1										
ME2/1	8.4	8.4	8.4	8.4	6.8	6.8	6.8	6.8	6.8	6.8	6.8	6.8	8.4	8.4
ME3/1	8.4	8.4	6.8	6.8	6.8	6.8	6.8	6.8	6.8	6.8	8.4	8.4		
ME4/1														

After setting the DAC2 codes, test strips are pulsed with large amplitudes and new T(i) are measured per each wire group. The newly measured T(i) and compared to pre-determined delays. Standing out sections of 8 wire groups would signal either cable connection mix-up or cables of incorrect length.

Available histograms:

hid = 1	distribution of average hit times after equalization
hid = 100 * layer + wiregroup	average delay time and error vs delay setting

Results:

`test_14_01.result` `test_14_01.ps`	`Result 1: Chisq(i) of the linear fit vs (plane, wire#)`
`test_14_02.result` `test_14_02.ps`	`Result 2: Delay slopes slope(i) ns/DAC vs (plane, wire#)`
`test_14_03.result` `test_14_03.ps`	`Result 3: Codes DAC1(i) to equalize delays for AFEB test pulse vs (plane, wire#)`
`test_14_04.result`	`Result 4: Slope(chip) in ns/DAC vs chip`
`test_14_05.result`	`Result 5: DAC1(chip) codes to equalize all delays for AFEB test pulses vs chip`
`test_14_06.result` `test_14_06.ps`	`Result 6: (DAC1(i)-DAC1(chip))*slope(i) for AFEB test pulse (ns) vs (plane, wire#)`
`test_14_07.result`	`Result 7: DAC2 codes to equalize all delays for muons vs (chip)`
`test_14_08.bad`	`Bad channels: (plane, wire#)  R1  R2  R3  R6 problem_code   #comment`
`test_14_09.result` `test_14_09.ps`	`Result 8: delay of the test strip pulse (ns) at the optimal DAC2(chip) with respect to the expected delay vs. (plane, wire#);`
`test_14_10.bad`	`Bad channels: (plane, wire#)  R9   problem_code   #comment`

Test 15. CFEB DAQ-Path Noise

Purpose: Measure CFEB pedestals, their stability (from one SCA cell to another, from one time sample to another, drift over ~10 hours) and all-inclusive noise for each strip. Check SCA block occupancy.

Method: Take data with a random (software) trigger[13]. Calculate the pedestal of each strip (all-inclusive: one entry for each event and each time sample), of each SCA capacitor of each strip, of each timesample of each strip). Calculate all-inclusive RMS, RMS of SCA pedestals, RMS of timesample pedestals. The last measurement evaluates contribution of cross-talks synchronous with read-out.

The run is repeated at low trigger frequency overnight: bad RMS of all-inclusive pedestals averaged over short-term periods is an indication of substantial drifts.

Analysis Details: The analysis makes three passes through the data. In the first two passes, it fills pedestal histograms, one histogram per strip, one entry per timesample. The first pass histograms have the full 4096 ADC count range and are used to find the pedestals approximately. The second pass histograms have a range of the mean value +- 100 ADC counts and are used to calculate mean and rms for each strip. The mean and rms are calculated using the peak bin +-10 ADC counts (is it too small?---it limits “measured” rms to ~20/srt(12)~6???)

Third pass: (I do not understand this part) A histogram of SCA block occupancy is filled. It is the occupancy of the first strip on each CFEB for layer 1. For each strip, the histogram is filled with one entry with weight 0.125 per timesample.

To allow one to check pedestal structure, for each strip, profile histograms are filled: ADC value vs SCA capacitor (1-96), vs timesample number (1-16), and vs event number. All ADC values are pedestal-subtracted, using the pedestals from pass 2.

Available histograms:
hid = 1 SCA Block occupancy
hid = 2 chisq/dof distribution for fit of pedestal vs event_number
hid = 1000 + 100 * layer + strip pedestal mean vs capacitor number
hid = 2000 + 100 * layer + strip pedestal mean vs timesample
hid = 3000 + 100 * layer + strip pedestal mean vs event_number

Results:

test_15_01.result test_15_01.ps	Result 1: All-inclusive pedestal vs (plane, strip#)
test_15_02.result test_15_02.ps	Result 2: All-inclusive RMS vs (plane, strip#)
test_15_03.result test_15_03.ps	Result 3: RMS of SCA cell pedestals vs (plane, strip#)
test_15_04.result test_15_04.ps	Result 4: RMS of timesample pedestals vs (plane, strip#)
test_15_05.result test_15_05.ps	Result 5: Long-term RMS of short-term all-inclusive pedestals vs (plane, strip#)
test_15_06.bad	Bad channels: (plane, strip#) R1 R2 R3 R4 R5 problem_code #comment

---

[13] Note that only 64 out of 96 SCA cells are accessible in the old-DAQ setup.

Test 16. CFEB Connectivity

Purpose: Check that all cathode preamps are connected to strips.

Method: Use ALCT test pulse generator to apply maximum amplitude test pulses to all wire groups of all layers simultaneously, which induces signals directly to strips due to capacitive coupling between wires and strips. AFEBs must be turned off (via ALCT) to achieve the maximum effect. Check the response of each strip to verify connectivity.

Analysis details: The software just checks that the response of each strip is of the right size. To check, it first makes a preliminary pass through the data to find which SCA bin usually has the peak amplitude, and which usually has the minimum amplitude. Then in the second pass it finds the average and rms of the difference of the values in these two bins (i.e. max - min). The same two bins are used for all strips. For each channel, <max-min> is required to be within the predefined range. The rms is used only for plotting.

Available histograms:

hid = 1 time bins with minimum amplitude

Results:

`test_16_01.result` `test_16_01.ps`	`Result 1: Max-Min in ADC counts (plane, strip#)`
`test_16_01.bad`	`Bad channels: (plane, strip#)  R1   problem_code   #comment`

Test 17. CFEB DAQ-Path Calibration

Purpose: To check the response of CFEBs on test pulse and measure calibration parameters and check that they are within specifications.

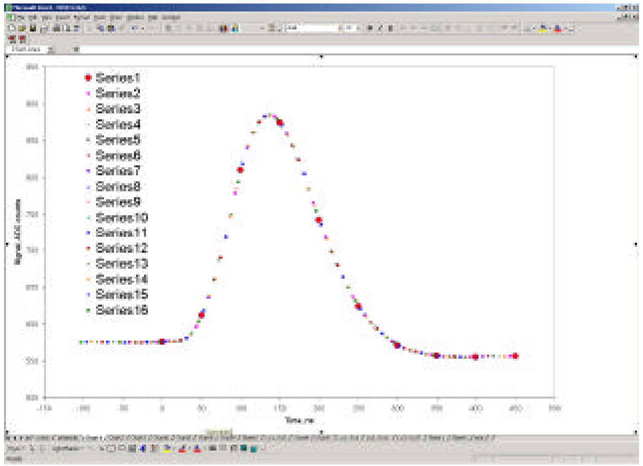
Method: Use the DMB test pulse generator to generate strip calibration signals. Two data files are written. The first file contains a scan over test pulse delays[14]. The second data file is a scan over test pulse amplitudes. The first scan allows one to measure: Buckeye gain for fixed Qin, uniformity of output pulse timing, pulse shape uniformity, cross-talk levels in nearby and far-away strips. The amplitude scan data is used to calibrate Buckeye's Q_output-vs-(Qin DAC): linear fit for slope and intercept. Non-linearity of the Buckeye response is also quantified.

Details:

Use the DMB test pulse generator to generate calibration signals by pulsing one strip at a time in each CFEB and layer (5 CFEBs * 6 layers = 30 strips are pulsed simultaneously).

Delay scan:

We pulse strips with Qin=100 fC (DAC code XXX) and find the average output pulse shape by histogramming distributions of mean ADC for 10 time samples for each of 16 test pulse delays[15]. Then, the pulse shape measurements are properly ordered in time, which gives a pulse shape in all details—see illustration in the figure.



Time corresponding to the peak is recorded for each strip: T(i). We check that output pulses on all strips appear at approximately the same time, i.e. we check $\Delta T(i)=T(i)-\langle T\rangle_{CSC}$ to be within acceptable limits.

Peak value minus pedestal (the left-most measurement of signal shape curve) is recorded for each strip: Apeak(i). We want to have spread of Apeak(i) to be within prescribed limits.

Sum of five SCA samples (+/-2 samples around the peak sample for the delay corresponding to the delay that gave Apeak(i): Q(i). Deviation of Q(i)/Apeak(i) from the value expected from the nominal pulse shape will signal us that the pulse shape is seriously distorted.

Left-side crosstalk is defined as the ratio LXT(pulsed-strip)=Apeak(left-neighbor-strip)/Apeak(pulsed-strip). Similarly is defined a Right-side crosstalk, RXT(i). Typical value for nearby strip crosstalks is ~10% and depends on a chamber type (strip width and length).

Long-Range crosstalk is defined as the ratio LRXT(i) = Amin(i)/(sum of Apeak(j) of all pulsed strips in a plane). Since normal long-range crosstalk goes through wires, it is negative.

---

[14] DAQMB-1999 provides steps are 6.89 ns/code. New DMB-2001 makes steps of ¼ of 25 ns clock, i.e. 6.25 ns/code.

[15] With the new DMB-2001, one needs not go beyond 8 steps in delay (the new DMB generates steps of exactly of 1/8 of the 50 ns clock used in SCA sampling)

Linearity:

We make a scan by pulsing strips with test pulses corresponding to DAC values (DMB-1999) from 0 to 250 with step of 10[16] and measure Q(i) for all pulsed strips. Then, a linear fit of Q vs DAC code is performed (slopes and intercepts are plotted). Fit is done in the range of DAC steps so that Amax<2000 by minimizing chi2 calculated using error weights corresponding to σ=sqrt(10^2+(0.01*ADC)^2), where 10 is a typical Q-integral noise of Buckeye chips[17]. Such defined weights equalize “badness” of deviations δA from the fit at low amplitudes (deviations below noise do not matter) and large amplitudes (deviations below 1% of signal amplitude do not matter either, since the calibration cannot be done with a precision better than 1%). Finally, the “goodness” of linear fit is evaluated as RMS for measured points around the fit line: $\delta A/\sigma$).

```
Available histograms:
--------------------
FILE test_17pass0-peak.his:
ID = 1                        - timesample with peak

FILE test_17_delay_scan.his [NOTE: i=1..5 - layer number, j=1..80 - strip number]

ID = (1000 + 100*i + j)               - pulsed strip signal shape (ampl. vs time)
ID = (2000 + 100*i + j)               - left strip crosstalk shape (ampl. vs time)
ID = (3000 + 100*i + j)               - right strip crosstalk shape (ampl. vs time)
ID = (10000 + 100*i + j)              - long-range crosstalk shape (ampl. vs time)

FILE test_17_dac_scan.his:
ID = (4000 + 100*i + j)               - charge Q vs DAC
ID = (5000 + 100*i + j)               - delta (Q – linear fit) vs DAC
```

---

[16] New DMB-2001 has 16 times finer DAC bits. Correspondingly the scanning parameters have to be changed.

[17] Noise per SCA sample is typically 3 ADC counts. With 0-correlation between 5 samples in the sum, the Q-noise would be $3\sqrt{5}=6.7$ counts, and with 100%-correlation—3×5=15. The reality is in between, ~10 counts.

Results:

test_17_01.result test_17_01.ps	Result 1: Output signal time offsets ΔT vs (plane, strip#)
test_17_02.result test_17_02.ps	Result 2: Output signal amplitudes Apeak for Qin=100 fC vs (plane, strip#)
test_17_03.result test_17_03.ps	Result 3: Output signal shape distortion: Q(ADC sum) / Apeak vs. (plane, strip#)
test_17_04.result test_17_04.ps	Result 4: Left-Side Crosstalk vs (plane, strip#)
test_17_05.result test_17_05.ps	Result 5: Right-Side Crosstalk vs (plane, strip#)
test_17_06.result test_17_06.ps	Result 6: Long-Range Crosstalk vs (plane, strip#)
test_17_07.bad	Bad channels: (plane, strip#) R1 R2 R3 R4 R5 R6 problem_code[18] #comment
test_17_08.result test_17_08.ps	Result 8: Q (ADC sum) vs DAC slope vs (plane, strip#)
test_17_09.result test_17_09.ps	Result 9: Q (ADC sum) vs DAC intercept vs (plane, strip#)
test_17_10.result test_17_10.ps	Result 10: Goodness of fit linearity vs (plane, strip#)
test_17_11.bad	Bad channels: (plane, strip#) R8 R9 R10 problem_code[19] #comment

---

[18] Problem codes: ΔT out of range: -25 ns to 25 ns
Apeak out of range (100 to 300 ADC counts)
Pulse distortion (1.6 to 2.5)
Left Crosstalk out of range (0 to 0.2)
Right Crosstalk out of range (0 to 0.2)
Long-Range Crosstalk out of range (<-0.01 or >0.01)

[19] Problem codes: Slope out of range: (XXX)
Intercept out of range (XXX)
Linearity is out of range (XXX)

Test 18. CFEB-Comparator Counting Noise:

Purpose: This test looks for noisy comparators.

Method: Take data in CLCT self-trigger mode, with only one layer required (i.e., a single-hit trigger). Measure the trigger rate of each strip. The test is done three times: HV=3600 V, and 3800 V.

Analysis details: Test for noise by triggering on single comparator hits (CLCT self-trigger mode). The comparator threshold is to be set for the nominal 15 fC threshold DAC (50 mV) Strip and halfstrip occupancy histograms get one entry per hit. There is a correction for DAQ deadtime: the rate is multiplied by the ratio of the number of ungated triggers to the number of events taken by the DAQ.

The test is done two times for different HVs. The software has no way to know the HV status automatically, so it asks the operator during the test. Results are plots of rates vs strip for HV=3600 and 3800 V, and a list of channels with rates outside the predetermined ranges.

```
Available histograms:
--------------------
file test18.root
six histograms (1 per layer)  corrected rate of comparator hits vs strip
six histograms (1 per layer)  corrected rate of comparator hits vs halfstrip
```

Results:

test_18_01.result test_18_01.ps	Result 1: Counting rate (plane, strip#) in Hz at HV=3600
test_18_02.result test_18_02.ps	Result 2: Counting rate (plane, strip#) in Hz at HV=3800 V
test_18_03.bad	Bad channels: (plane, strip#) R1 R2 problem_codes[20] #comment

---

[20] Problem codes:
Low/High Rate at HV=3600 (5 - 40 Hz)
Low/High Rate at HV=3800 (5 - 80 Hz)

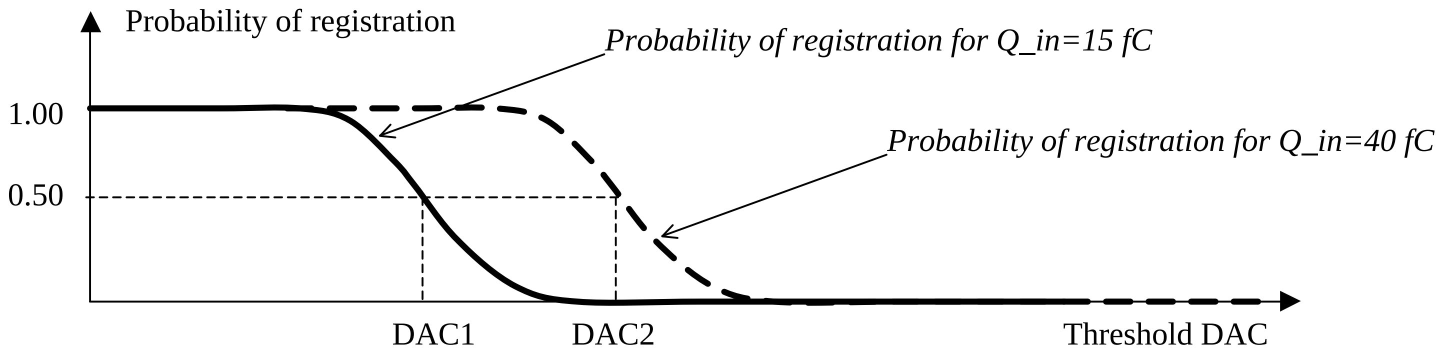
Test 19. CFEB-Comparator Thresholds and Analog Noise

Purpose: To measure the offsets and noise of the threshold comparators in the comparator chips.

Method: Uses the DMB test pulse generator to apply calibration pulses (single-strip pulses) to one channel at a time of each Buckeye chip (5 CFEBs * 6 layers are pulsed simultaneously). The test pulse amplitude is fixed at DAC1=23[21] (code for Q_in~15 fC). The threshold is scanned in 35 steps of 3 mV starting from 13 mV[22]. Turn-off curve (efficiency vs mV) is fit with an error function for the 50% efficiency point and comparator analog noise (fit sigma)[23]. The best DAC1 (in mV) value (average, excluding outliers??) is picked for each CFEB board. The scatter of channel threshold offsets (in mV) within a board is checked.

The procedure is repeated for pulse amplitude set at DAC1=61 (code for Q_in~40 fC) and threshold scan starting point of 49 mV to yield results analogous to the first scan.

Combination of the results from the two scans gives threshold(mV)-vs-Q_in slopes, (DAC2-DAC1)/(40 fC - 15 fC), per channel and per board.



---

[21] The numbers given in this description are for DMB-2001. The DMB-1999 has 10.5 fC/count for the calibration pulse amplitude and is claimed to have a substantial non-linearity. If one takes Buckeye chip to be linear at small amplitudes, setting of 2 DAC bits seems to correspond approximately to 16.5 fC. Therefore, we can take codes 2 and 5 for thresholds 15 fC and 40 fC.

[22] Currently (DMB-1999), the FAST-DAQ is set up to make a scan of 35 steps, 3 mV each, starting from DAC1*12-11.

[23] Due to occasional fit instabilities, this procedure is replaced by measuring mean and RMS of the histogram obtained by differentiating the turn-off histogram.

Analysis details: A histogram of the number of events with a hit vs threshold is filled for each strip channel. There is no particular requirement on the hit time, only that it be within the readout window of ?? clocks. Each histogram is then differentiated, the mean(i) of the new histogram is the threshold corresponding to 50% efficiency, DAC1(i), and the rms(i) is the comparator analog noise, both measured in threshold mV. Failure to find mean and/or rms is flagged with error code –1. For each board, an average of DAC1(i) values is taken, after excluding bad channels. This value DAC1(board) is to be used for data taking. The spread of DAC1(i) values around DAC1(board) is checked.

Analysis is repeated for CFEB test pulse signal setting corresponding to 40 fC. Slope is measured as (DAC2 – DAC1)/(40 fC - 15 fC). Channels tagged as bad in either 15 fC or 40 fC test signal runs will have slope set to –1 (no calculations of slope are performed).

Available histograms include:

10000 * scan + 1000 + ilayer	strip occupancy
10000 * scan + 1000 + 100 + 5*(ilayer-1) + cfeb	time bins occupancy per chip
10000 * scan + 1000 + 200 + 5*(ilayer-1) + cfeb	calibration pulse DAC
10000 * scan + 2000 + 100*ilayer +istrip	time bins occupancy
10000 * scan + 3000 + 100*ilayer + istrip	turn-off curve (threshold is in sequential steps of measurements, NOT in mV)

Results:

test_19_01.result	Result 1: DAC1(CFEB) threshold (mV) for 50% efficiency at Qin=15 fC vs. CFEB#
test_19_02.result test_19_02.ps	Result 2: Threshold offsets DAC1(i)-DAC1(CFEB) in mV vs. (plane, strip#) for 15 fC
test_19_03.result	Result 3: DAC2(CFEB) threshold (mV) for 50% efficiency at Qin=40 fC vs. CFEB#
test_19_04.result test_19_04.ps	Result 4: Threshold offsets DAC2(i)-DAC2(CFEB) in mV vs. (plane, strip#) for 40 fC
test_19_05.result test_19_05.ps	Result 5: Threshold slopes(i) in mV/fC vs. (plane, strip#)
test_19_06.result	Result 6: Threshold slopes(CFEB) in mV/fC vs. CFEB#
test_19_07.bad	Bad channels: (plane, wire#) R2 R4 R5 R8 R9 R10 R11 problem_code[24] #com’t
test_19_08.result test_19_08.ps	Result 8: Noise(i) in fC at threshold=15 fC vs (plane, strip#)
test_19_09.result test_19_09.ps	Result 9: DAC1(i) for threshold=15 fC vs (plane, strip#)
test_19_10.result test_19_10.ps	Result 10: Noise(i) in fC at threshold=40 fC vs (plane, strip#)
test_19_11.result test_19_11.ps	Result 11: DAC2(i) for threshold=40 fC vs. (plane, strip#)

Examples:

```
Test 19: Comparator Threshold and Analog Noise Test
test_19_03.result: Optimal DAC1 values (mV) per CFEB for 15 fC threshold
ME234/2-034
Test performed:  15-Nov-2001  UC Ignatenko    DAQ-1.50
Analysis done:   15-Nov-2001  Analysis-2.00
FAILED, -Ignatenko

CFEBs
 1  xxx
 2  xxx
 3  xxx
 4  xxx
 5  xxx
```

---

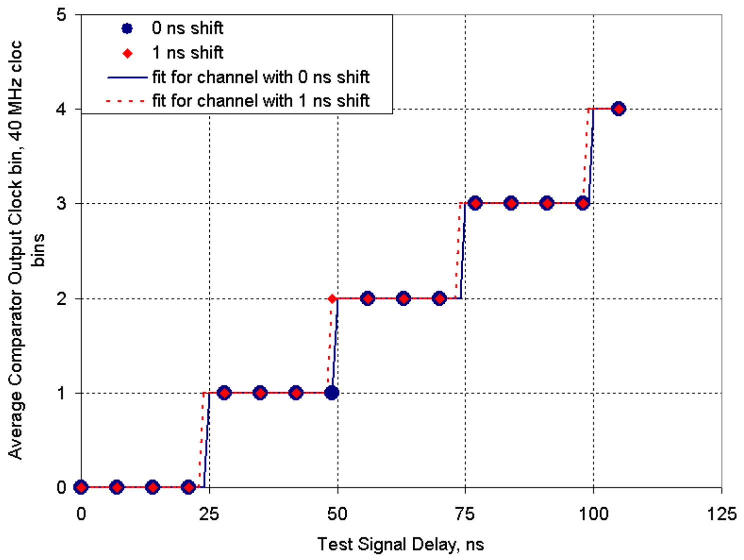
[24] Problem codes: RMS at 15 fC out of range
DAC2(15 fC) out of range
Delta_DAC2(15 fC) out of range
RMS at 40 fC out of range
DAC2(40 fC) out of range
Delta_DAC2(40 fC) out of range
mV/fC slope out of range

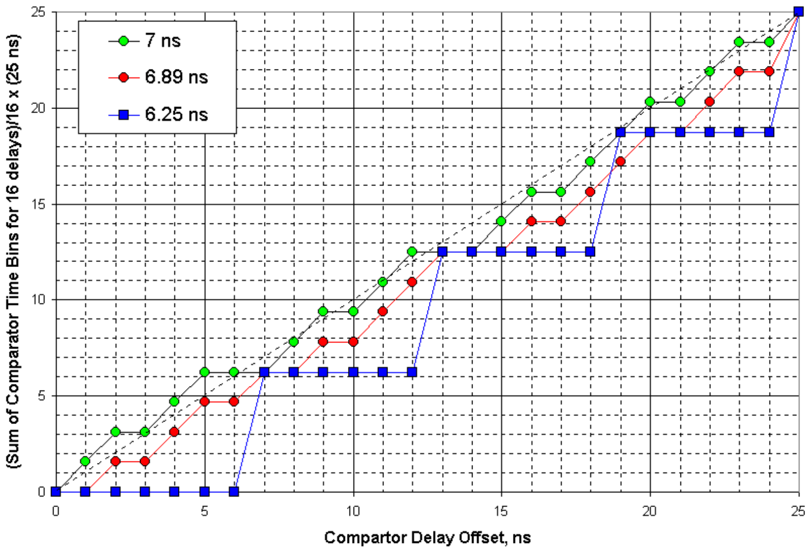
Test 20. CFEB-Comparator Output Timing

Purpose: This test is designed to check the simultaneity of the comparator outputs.

Method: Uses the DMB test pulse generator to apply calibration pulses (single-strip pulses) to one channel at a time of each Buckeye chip (5 CFEBs * 6 strips are pulsed simultaneously). The pulse amplitude is fixed at 150[25] DAC1 counts, or Q_in~100 fC, and the pulse delay is scanned from 0 to 15 * 6.25 ns[26], resulting in a 4-time-bin range for the comparator hits. For each channel, profile histograms are made of the average comparator time bin vs delay. In case of no time jittering, the plots would look like perfect staircases—see the picture below where results for two channels with 1 ns time offset are plotted together with a staircase fit (plots are for DMB-1999 that had about 7 ns per delay step). The natural jitter due to electronics noise makes steps smoother than those shown in the picture, which actually allows for better determination of relative time shifts of the staircase-like plots corresponding to different channels. One could fit the staircase with a set of staggered error-functions. However, we chose a simpler and more robust way: one can find the center of gravity of all 16 points as projected on Y-axis. The center of gravity turns out to follow the time offsets with quite good precision: ~1 ns for the old DMB-1999 with 7 ns steps; and with no more than 6.25 ns error for DMB-2001 with steps of exact ¼-th fraction of 25 ns (see picture below).

In general, time non-uniformity may be caused not only by intrinsic faults in the comparator timing logic, but also by non-uniformity of the comparator thresholds and test pulse shapes.





---

[25] The number is given for DMB-2001. Same charge for DMB-1999 would correspond to DAC1=12.

[26] 6.25 ns is the step for DMB-2001. DMB-1999 should have steps of 6.89 ns as measured with actual boards (7 ns in the design specs).

Analysis details: Time offsets are calculated with respect to the average per CFEB.

```
Available histograms:
--------------------
file test0.his
hid = layer                         comparator hit occupancy vs strip
hid = 10                            fit chisq
hid = 11                            offset
hid = 12                            offset error
hid = 13                            sigma
hid = 14                            sigma error
hid = 1000 + 100 * layer + strip    profile hist, comparator bin vs pulse delay
```

Results:

test_20_01.result test_20_01.ps	Result 1: Comparator time offsets (ns) vs. (plane, channel)
test_20_02.bad	Bad channels: (plane, strip) R1 problem_code[27] #comment

---

[27] Problem Codes: Large time offset (\|offset\| > 25 ns)

Test 21. CFEB-Comparator Logic

Purpose: To check the half-strip logic and the trigger test pulse system.

Method: Use DMB test pulse generator to apply trigger test pulses to three adjacent strips at a time in each CFEB and layer (3*5*6 strips are pulsed simultaneously). The three strips have amplitudes in the ratio 1:3:2 or 2:3:1, and each half-strip is selected in turn by looping over triplets of strips and alternating between the two ratios. The test pulse amplitude is set at DAC1=25 code for DMB-2001 or 2 code for DMB-1999, which corresponds approximately to 60, 120, and 180 fC charges on the three strips.

Analysis details: One collects occupancy histograms (number of entries vs half-strip number) for N triggers per half strip and measures fractions (or efficiencies) of correct responses vs half-strip. Note that the fraction may be greater than 1.0 if the half-strip also responses on pulses that were set to trigger other half-strips.

Results:

test_21_01.result test_21_01.ps	Result 1: Efficiency vs. (plane, halfstrip#)
test_21_02.bad	Bad channels: (plane, halfstrip#) R1 problem_code[28] #comment

---

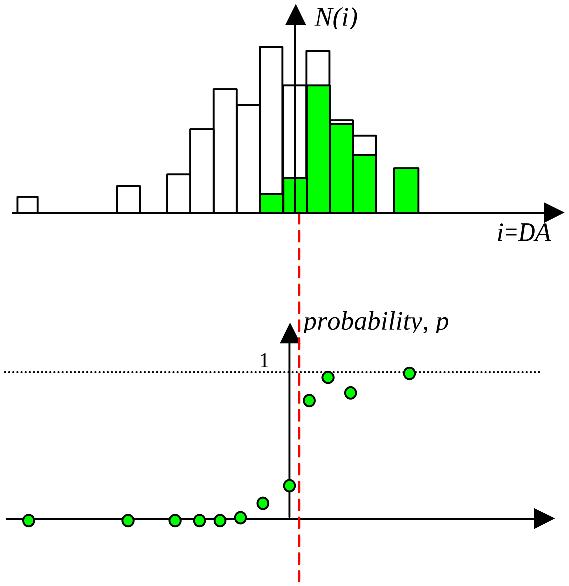
[28] Problem Codes: Dead (efficiency < 0.05)
Low Efficiency (efficiency <0.90)
High cross-talk (>1.10)

Test 23. CFEB-Comparator Input Offsets

Purpose: To measure the offsets and noise of the "neighbor strip" comparators, (n+1) vs. (n), and left/right neighbor comparators, (n+1) vs. (n-1).

Method: Uses scintillator-triggered cosmic data[29]. The analysis looks in the data for comparator hits and plots probability for a particular comparator channel to be on/off vs signal amplitude difference (in pedestal-subtracted ADC counts) between two strips being compared. The curve of probability is fit with an error function to find the turn-over point and analog noise level (fit sigma).

Analysis details: The analysis makes two preliminary passes through the data to measure the pedestals. It makes two ΔA=A(n+1)-A(n) occupancy histograms: one with the left-hand halfstrip selected on the right-hand strip in the pair (green in figure), and one with either halfstrip selected (right-hand halfstrip on the left strip in the pair or left-hand halfstrip on the right strip in the pair, white in figure). Amplitudes are taken at time bin corresponding to the peak of the largest signal. The ratio of these two histograms is the fraction of left-hand comparator hits on the right strip vs ΔA. We use the error-function fit to find the turn-over point and noise level. Absolutely the same analysis is done for comparing (n+1) vs (n-1) strips, i.e. for probability of finding left/right half strip vs amplitude difference on left/right neighbor-strips, ΔA=A(n+1)-A(n-1).



Bad channels are those which fail cuts on offset or have too little statistics (an indication of low efficiency or scintillator trigger problems).

Results:

test_23_01.result test_23_01.ps	Result 1: (N+1)-(N) offset in ADC counts vs. (plane, strip#)
test_23_02.result test_23_02.ps	Result 2: (N+1)-(N) noise in ADC counts vs. (plane, strip#)
test_23_03.result test_23_03.ps	Result 1: (N+1)-(N-1) offset in ADC counts vs. (plane, strip#)
test_23_04.result test_23_04.ps	Result 2: (N+1)-(N-1) noise in ADC counts vs. (plane, strip#)
test_23_05.result test_23_05.ps	Result 3: Number of events vs. (plane, half-strip#)
test_23_06.bad	Bad channels: (plane, strip#) R1 R2 R3 R4 R5 problem_code[30] #comment

---

[29] Unlike the left/right test, we have to have a signal on the strips examined by the comparators, otherwise there will be nothing over threshold and nothing read out. On the other hand, the DMB-CFEB design does not allow one to do this measurement using test pulses. So, the test is done with scintillator-triggered cosmic data.

[30] Problem Codes: Large offset (|offset|> XXX); Low/Large noise (<XXX or >XXX); Low Statistics (N < XXX)

```
Available histograms:
--------------------
file test.his
hid = 1                               chisq distribution
hid = 2                               offset error distribution
hid = 3                               noise error distribution
hid = 100 * layer + strip             dQ distribution, left halfstrip comp. on
hid = 1000 + 100 * layer + strip      dQ distribution, left or right comp. on
hid = 2000 + 100 * layer + strip      dQ, 1 + fraction with left comp. on
```

Test 24. Absolute Gas Gain Map (with cosmic rays)

Purpose: Check chamber gain and find voltage offsets for each HV segment to equalize the gas gain.

Method: Use cosmic data to make Landau plots. HV=3600 V for all planes. An online filter requiring that an LCT was found by the CLCT and that the scintillator pattern is "from the interaction region" plus or minus one scintillator-width is used to increase the fraction of useable events.

Analysis details: To check the chamber gas gain uniformity, the gain is measured separately in sub-plane regions defined as (1 CFEB) x (1 HV segment). ME234/2 have 5x5=25 regions per plane, ME234/1 and ME1/2 chambers --- 5x3=15 regions, ME1/3 chambers --- 4x3=12 regions. ALCT key-wire-groups are used to assign tracks to one or another HV segment. There is also a primitive track-finding in the strip view, intended to select more-or-less vertical tracks. It finds the largest cluster in each layer, and requires that the difference in the strip number between the top and bottom clusters be no more than 2 strips / layer[31]. Clusters on the boundary between two CFEBs are excluded from the Landau plots (the cluster peak can't be on the first or last strip of a CFEB).

The chamber gain is measured by fitting histograms of the charge distribution of clusters with the Landau function (from CERNLIB). Cluster charge is defined as the sum of 25 samples: 5 time samples from each of 5 strips, centered on the peak ADC value. Pedestals are calculated event-by-event from the first 3 SCA samples. The fit with the Landau function is preceded by a fit with a Gaussian, which supplies starting parameters for the Landau fit.

Deviation of mean cluster charge for each of the HV segments from the nominal Q_0=XXX for 3600 V is calculated: $r=(<Q>-Q_0)/Q_0$. Corrections for HV are calculated from the exponential dependence of charge on HV: $Q=Q_0\exp(\alpha\cdot\Delta HV)$, where $\alpha=0.00533\ V^{-1}$. This results in $\Delta HV=-\ln(r)/\alpha$ in Volts.

Results:

test_24_01.result test_24_01.ps	Result 1: Landau peak vs. (plane, “x”), where “x” = CFEB + 5 * (HV segment – 1)
test_24_02.result	Result 2: HV offsets (V) vs. (plane, HV segment#)

```
Available histograms include:
-----------------------------
file test.his
hid = layer              max 5-bin adc sum
hid = 10 + layer         strip with max 5-bin sum
hid = 20                 peak time bin of strip with max 5-bin sum
hid = 21                 peak time bin of strip with max 5-bin sum > 100
hid = 22                 track slope in stripwidths/layer
hid = 23                 track x in stripwidths
hid = 24                 distribution of Landau peaks
hid = 25                 chisq of Landau fit
hid = 100 * layer + 10 * HV segment + cfeb     Landau plots (5x5 adc sum)
```

---

[31] This selection slightly biases the results by accepting larger-angle tracks in the wide end of the chamber.

Test 25. ALCT Self-Trigger

Purpose: Check the ALCT trigger rate at different conditions.

Method: Check the ALCT0 rates for each key wire group for 1-of-6, 2-of-6, 3-of-6, 4-of-6, 5-of-6, and 6-of-6 plane coincidence requirements. Repeat the same measurement after placing a Cs radioactive source (no changes in rates for 3-of-6 and above are expected). Measure 4/6-ALCT0 rate, 4/6-ALCT1 rate, average 4/6-ALCT-quality, and number of raw hits vs. high voltage.

Details: The DAQ is set up to be triggered by the ALCT, and to scan over the required number of planes in coincidence. The scan settings are 1-1, 2-2, 2-3, 2-4, 2-5 and 2-6, with equal numbers of events, where in m-n, m is the number of planes required to pre-trigger, and n is the number required to trigger. The nominal setting is 2-4. The trigger rate falls off as n is increased because of reduced background from random hits (strongest effect as n goes from 1 to 2) and because the accepted incidence angle is reduced as more layers are required. The test produces a plot of trigger rates. The trigger rates are corrected for DAQ dead-time if there is scaler data available giving the ungated ALCT trigger rate. (Otherwise, it prints a warning message and the rates are not corrected.) The correction is just to multiply the measured rate by num_ungated_triggers / num_events. In the plots, the rates are normalized by the wire group length (so what's plotted is Hz/meter of wire length) so that they are expected to be equal for all wire groups.

A second datafile is taken with a chamber exposed to Cs source. The DAQ and analysis are exactly the same. One expects to see a large bump in 1/6-ALCT0 rates, but no noticeable changes in 3/6-ALCT0 and above rates.

Results:

test_25_01.result test_25_01.ps	Result 1: m/6-ALCT0 rate vs. (m, key wire group#) at normal conditions
test_25_02.result test_25_02.ps	Result 2: m/6-ALCT0 pattern quality vs. (m, key wire group#) at normal conditions
test_25_03.result test_25_03.ps	Result 3: m/6-ALCT0 rate vs. (m, key wire group#) with Cs source
test_25_04.result test_25_04.ps	Result 4: m/6-ALCT0 pattern quality vs. (m, key wire group#) with Cs source
test_25_04.bad	Bad channels: (plane, strip#) R1 R3 problem_code[32] #comment

```
Available histograms:
--------------------
file test0.his
hid = 10 + nplanes    number of LCTs found vs key wiregroup
hid = 20 + nplanes    average pattern quality vs key wiregroup
hid = 30 + nplanes    number of accelerator muons found vs key wiregroup
```

---

[32] Problem Codes: Large/Low Rate for 4/6-ALCT0

Test 26. CLCT Self-Trigger

Purpose: Check the CLCT trigger rate at different conditions.

Method: Check the CLCT0 rates for each key half-strip for 1-of-6, 2-of-6, 3-of-6, 4-of-6, 5-of-6, and 6-of-6 plane coincidence requirements. Repeat the same measurement after placing a Cs radioactive source (no changes in rates for 3-of-6 and above are expected). Measure 4/6-CLCT0 rate, 4/6-CLCT1 rate[33], average 4/6-CLCT-quality[34], and number of raw hits vs. high voltage.

Details: The DAQ is set up to be triggered by the CLCT, and to scan over the required number of planes in coincidence. Write a data file with six different trigger conditions (pattern/plane trigger thresholds = 1/1, 2/2, 2/3, 2/4, 2/5, and 2/6). The threshold-settings are a screwdriver adjustment; the run will pause automatically when they need to be changed. The trigger rate falls off as n is increased because of reduced background from random hits (strongest effect as n goes from 1 to 2) and because the accepted incidence angle is reduced as more layers are required. The test produces a plot of trigger rates. The trigger rates are corrected for DAQ dead-time if there is scaler data available giving the ungated CLCT trigger rate. (Otherwise, it prints a warning message and the rates are not corrected.) The correction is just to multiply the measured rate by num_ungated_triggers / num_events.

A second datafile is taken with a chamber exposed to Cs source. The DAQ and analysis are exactly the same. One expects to see a large bump in 1/6-CLCT0 rates, but no noticeable changes in 3/6-CLCT0 and above rates.

Results:

test_25_01.result test_25_01.ps	Result 1: m/6-CLCT0 rate vs. (m, half-strip#) at normal conditions
test_25_02.result test_25_02.ps	Result 2: m/6-CLCT0 pattern quality vs. (m, half-strip#) at normal conditions
test_25_03.result test_25_03.ps	Result 3: m/6-CLCT0 rate vs. (m, half-strip#) with Cs source
test_25_04.result test_25_04.ps	Result 4: m/6-CLCT0 pattern quality vs. (m, half-strip#) with Cs source
test_25_04.bad	Bad channels: (plane, strip#) R1 R3 problem_code[35] #comment

```
Available histograms:
--------------------
file test0.his
hid = 10 + nplanes    number of LCTs found vs key half-strip
```

---

[33] Not available with DAQ based on 1999 boards.

[34] Not available with DAQ based on 1999 boards.

[35] Problem Codes: Large/Low Rate for 4/6-CLCT0

Test 27. High Statistics Cosmic Ray Test

Purpose: Measure plane misalignment, chamber performance (resolution and efficiency), and do various tests that couldn't be done any other way.

Method: Use the scintillators to trigger on cosmics. Data is filtered to get the best possible sample of tracks at "LHC" angles.

Details: The analysis makes four passes through (at least some of) the data for this test. The first and second passes are primarily to find the pedestals. The third pass is used to do "first pass" track-fitting and get the layer alignment constants. Finally, the last pass uses the alignment constants and calculates the strip resolution. Tests that don't need tracks are mostly done in pass 2, and those that do rely on tracking are done in pass 3.

The number of events is limited to 129k by the maximum allowed file size. So, the data is filtered online to get the highest possible fraction of useable events ("high-momentum" tracks). The filter must require only clean scintillator patterns (only one paddle at the top plane and only one paddle at the bottom plane) at the LHC-like angle. The filter is also to require at least one comparator hit, strictly speaking this compromises the efficiency calculation, but the effect should be very small.

Pass 0 and pass 1 are used to calculate pedestals from the first 50 and 5000 events respectively (if the pedestals drift significantly in the 6 hours it takes to take data, then this method will not give a good result). The pedestals used by the rest of the analysis are the mean of the second and third SCA samples of the first 5000 events.

Pass 2 begins with track-finding, first in the wire projection and then in the strip projection. In the wire projection, the track-finding uses the ALCT algorithm (to be replaced with real ALCT0 key wire group). Only events that have one good ALCT track (and thus have a track with a well-defined radial position) are used in the rest of the analysis.

The strip track-finding is done using the 1998 CLCT algorithm, because this algorithm works well even in the presence of a lot of background, so hopefully much of the code can be reused for test 24. Once an LCT track is found, cluster fitting is done in each layer on the strips where the track crosses it. (This works lots better than finding clusters with a peak-finding algorithm.) Then an unweighted linear fit is made to the clusters in all six layers, and the difference between the cluster position and the track position is histogrammed in each layer. This is the input to the alignment routine at the end of pass 2.

The disadvantage of using the LCT algorithms is that they tend to be quite slow, since they have to start (for the strips) by simulating comparator hits, and then look at all possible key halfstrips or wire groups. (In other words, they are slow because they do serially what the hardware does in parallel.)
To speed things up, the ALCT and CLCT track-finding results from pass 2 are saved in the file test_results/temp/xclusters.dat.

Profile histograms of long-range crosstalk for each CFEB and layer are also made in pass 2. These are separated into two sets of histograms.

In pass 3, the cluster fitting is repeated. (Although the cluster fits are unaffected by the alignment correction, the idea was to also do a distortion correction in pass 2 based on the uniformity of the cluster fit x-distribution. In this case it makes sense to also redo the cluster fit in pass 3. The distortion-correction algorithm just never got completed.) Then the track fit is redone (with alignment) and with weights from the cluster fit. Both 5- and 6-layer fits are done (ie the maximum number of layers used is 5 or 6). The 5-layer fit is used to measure clusterfit residuals and thence resolution, and the 6-layer fit is used to measure comparator performance. (This is why the comparator efficiency looks better than the clusterfit resolution!)

Strip resolution is plotted vs wiregroup number for 5 ranges of x, where x=0 means the track is centered on a strip, and x=0.5 means the track is centered between strips. For the resolution measurements, the track is required to have | phi | < 0.1 radians.

Results:
----

test_27_01.ps	plot of ALCT wire hit times (for hits assoc. with tracks)
test_27_02.ps	plot of mean halfstrip residuals (to check comparator offsets)
test_27_03.ps	plot of comparator efficiency (comp on within 0.5 stripwidths)
test_27_04.ps	plot of strip efficiency (cluster position within 0.5 stripws)
test_27_05.ps	long-range crosstalk, CFEB 1, track not in CFEB
test_27_06.ps	long-range crosstalk, CFEB 2, track not in CFEB
test_27_07.ps	long-range crosstalk, CFEB 3, track not in CFEB
test_27_08.ps	long-range crosstalk, CFEB 4, track not in CFEB
test_27_09.ps	long-range crosstalk, CFEB 5, track not in CFEB
test_27_10.ps	layer alignment plots and fits
test_27_11.ps	comparator efficiency numerator and denominator histograms
test_27_12.ps	strip efficiency numerator and denominator histograms
test_27_13.ps	strip resolution, 0.0 < | x | <= 0.1
test_27_14.ps	strip resolution, 0.1 < | x | <= 0.2
test_27_15.ps	strip resolution, 0.2 < | x | <= 0.3
test_27_16.ps	strip resolution, 0.3 < | x | <= 0.4
test_27_17.ps	strip resolution, 0.4 < | x | <= 0.5

```
Available histograms:
---------------------
Pass 0 (file test27_0.his):
  10                           LCT hit times (used as input to the alct simulation)
  100 + 10 * layer + strip     full ADC range ADC occupancy plot (for ped calc.)

Pass 1 (file test27_1.his):
  100 + 10 * layer + strip     reduced-range ADC occupancy plot (for ped calc.)

Pass 2 (file test27_2.his):
    1                          key wiregroup occupancy
    2                          key halfstrip occupancy
    3                          key distrip occupancy
   60 + laye                   Anode hit times (profile histogram)
 1000 + 100 * layer + wiregroup    Trackfit residual (for layer alignment)
  200 + 10 * layer + CFEB      long-range crosstalk in same cfeb as track
  600 + 10 * layer + CFEB      long-range crosstalk in cfebs without tracks
  300 + 10 * layer + CFEB      clusterfit x-profile (to monitor distortion)
  400 + 10 * layer + CFEB      clusterfit x-occupancy (for distortion correction?)
  500 + 10 * layer + CFEB      clusterfit x-occupancy, restricted phi angle
 4000 + 10 * layer + CFEB      plots for scintillator calibr. (for online filter)

Pass 3 (file test27_3.his):
  101                          trackfit chisq/ndf
  102                          number of layers in fit
  110 + layer                  clusterfit chisq
  120 + layer                  strip efficiency, numerator
  130 + layer                  strip efficiency, denominator
  140 + layer                  comparator efficiency, numerator
  150 + layer                  comparator efficiency, denominator
  160 + layer                  comparator residuals (compared to track position)
  170 + layer                  cluster charge (from cluster fit)
  300 + 10 * layer + CFEB      clusterfit x-profile (to monitor distortion)
 1000 + 100 * layer + wiregroup    trackfit residual (to check alignment)
20000 + 1000 * layer + 10 * wiregroup + HV segment
                               clusterfit residual (for resolution)
```

Test 28. ALCT and CLCT rate vs HV

Purpose: Measure plateau of ALCT and CLCT rates on cosmic rays

Method: Both ALCT and CLCT are programmed to trigger on 4/6 and rate of their decisions is measured vs HV with the help of plain scalers in the old DAQ (V1.X) and with the help of CCB in the new DAQ (V2.X).

Results:

test_28_01.result test_28_01.ps	Result 1: 4/6-ALCT and 4/6-CLCT rate (Hz) vs. HV at normal conditions

Example:

```
Test 28:            4/6-ALCT and 4/6-CLCT rate vs HV
test_28_01.result:  4/6-ALCT and 4/6-CLCT rate vs HV
ME234/2-034
Test performed:  15-Jun-2002  UC Ignatenko    DAQ-1.50
Analysis done:   15-Jun-2002  Analysis-2.00
OK, -Ignatenko

HV (kV)   ALCT (Hz)   CLCT (Hz)

3.2        20          1
3.25       50          1
3.3        113         4
3.35       214         11
3.4        309         29
3.45       358         61
3.5        378         99
3.55       386         129
3.6        387         141
3.65       391         149
3.7        398         155
3.75       398         153
3.8        398         154

# CLCT rate was taken with 50 mV threshold (higher than nominal)
```

Test 30. Gas Leak (before shipping to CERN)

Purpose: Detection of gas leaks

Method: Chamber is over-pressurized with gas to 3 inches of water column equivalent and the leak is evaluated based on the drop of the overpressure in 24 hours. Follow the note outlining the leak rate measurement procedure.

Results:

test_30_01.result	Result 1: List of results: Rate (cc/min), Overpressure at start (" H20), date, # brief com’t # Detailed comments, history of repairs (location, method of repairing, etc.)

Example:

```
Test 30:            Gas Leak Test (incoming)
test_30_01.result:  Gas leaks
ME234/2-034
Test performed:  15-Jun-2001  UC Ignatenko    DAQ-1.50
Analysis done:   15-Jun-2001  Analysis-2.00
OK, -Ignatenko

1.2    3.0   15-Jun-2001
```

Chamber Shipped to CERN-ISR

Purpose: Record the shipping date and any relevant comments.

Method: Use *"CSC/Electronics Inventory Database"*. This is applicable to all FAST Sites: UF, UC, PNPI, IHEP. The database automatically makes a report on which boards, being currently installed on this chamber, have been shipped to CERN.